Am1702A

256-Word by 8-Bit Programmable Read Only Memory

Advanced MOS/LSI

DISTINCTIVE CHARACTERISTICS

- Field programmable 2048 bit ROM
- Access times down to 550 nanoseconds
- 100% tested for programmability
- Inputs and outputs TTL compatible
- Three-state output – wired-OR capability
- Typical programming time of less than 2 minutes/device
- Clocked VGG mode for lower power dissipation
- 100% MIL-STD-883 reliability assurance testing

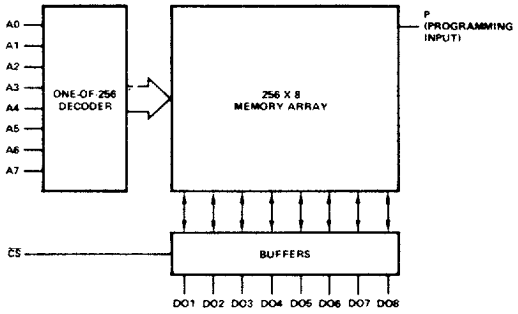
GENERAL DESCRIPTION

The Am1702A is a 2048 bit electrically programmable ultraviolet light erasable Read Only Memory. It is organized as 256 by 8 bits. It is packaged in a 24 pin dual in-line package with a transparent quartz lid, and is available in both hermetic and epoxy sealed packages.

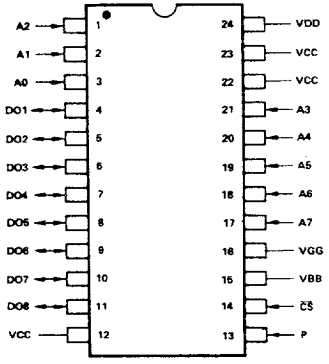
The transparent lid allows the user to erase any previously stored bit pattern by exposing the die to an ultraviolet (UV) light source. Initially, and after each erasure, all 2048 bits are in the zero state (output low). The data is selectively written into specified address locations by writing in ones.

A low power version, the Am1702AL, is available which permits the VGG input to be clocked for lower average power dissipation.

BLOCK DIAGRAM



CONNECTION DIAGRAM



Top View

Pin 1 is marked for orientation

ORDERING INFORMATION

Ambient Temperature Specification	Package Type	Clocked VGG	Access Time (ns)		
			1000	650	550
0°C to +70°C	Epoxy Seal	No	AM1702A	AM1702A-2	AM1702A-1
		Yes	AM1702AL	AM1702AL-2	AM1702AL-1
	Hermetic Seal	No	AM9702AHDC	AM9702A-2HDC	AM9702A-1HDC
		Yes	AM9702ALHDC	AM9702AL-2HDC	AM9702AL-1HDC

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Power Dissipation	1 W
Input and Supply Voltages (Operating)	VCC −20 V to VCC +0.5 V
Input and Supply Voltages (Programming)	−50 V

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE, Read Mode (Notes 1, 2)

Ambient Temperature	VCC	VDD	VGG	VBB
0°C to +70°C	+5.0V ±5%	−9.0V ± 5%	−9.0V ± 5%	+5.0V ± 5%

ELECTRICAL CHARACTERISTICS over operating range (Note 3)

Parameter	Description	Test Conditions	Am1702A Min.	Am1702A Typ.	Am1702A Max.	Am1702AL Min.	Am1702AL Typ.	Am1702AL Max.	Unit
ICF1	Output Clamp Current	T_A = 0°C, VO = −1.0V		8	14		5.5	8	mA
ICF2	Output Clamp Current	T_A = 25°C, VO = −1.0V			13		5	7	mA
IDD0	VDD Current (Note 4)	VGG = VCC, IOL = 0mA, $\overline{CS}$ = VCC −2.0, T_A = 25°C					7	10	mA
IDD1		IOL = 0mA, $\overline{CS}$ = VCC −2.0, T_A = 25°C		35	50		35	50	mA
IDD2		IOL = 0mA, $\overline{CS}$ = 0, T_A = 25°C		32	46		32	46	mA
IDD3		IOL = 0mA, $\overline{CS}$ = VCC −2.0, T_A = 0°C		38	60		38	60	mA
IGG	VGG Current				1.0			1.0	μA
IL1	Input Leakage Current	VI = 0V			1.0			1.0	μA
ILO	Output Leakage Current	$\overline{CS}$ = VCC −2.0, VO = 0V			1.0			1.0	μA
IOH	Output Source Current	VO = 0V	−2.0			−2.0			mA
IOL	Output Sink Current	VO = 0.45V	1.6	4		2.0			mA
VIH	Input HIGH Level		VCC−2.0		VCC+0.3	VCC−2.0		VCC+0.3	Volts
VIL	Input LOW Level		−1.0		0.65	−1.0		0.65	Volts
VOH	Output HIGH Level	IOH = −200μA	3.5	4.5		3.5	4.5		Volts
VOL	Output LOW Level	IOL 1.6mA		−3.0	0.45				Volts
		IOL 2.0mA						0.4	

SWITCHING CHARACTERISTICS over operating range (Note 5)

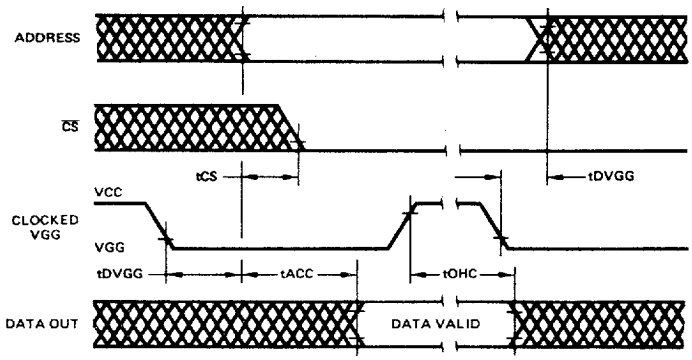
Parameter	Description	Am1702A-1 / Am1702AL-1 Min.	Am1702A-1 / Am1702AL-1 Max.	Am1702A-2 / Am1702AL-2 Min.	Am1702A-2 / Am1702AL-2 Max.	Am1702A / Am1702AL Min.	Am1702A / Am1702AL Max.	Unit
tACC	Address to Output Access Time		550		650		1000	ns
tCO	Output Delay from $\overline{CS}$		450		350		900	ns
t$\overline{CS}$	Chip Select Delay		100		300		100	ns
tDVGG	Set-up Time, VGG	0.3		0.3		0.4		μs
tOD	Output Deselect		300		300		300	ns
tDH	Previous Read Data Valid		100		100		100	ns
tOHC	Data Out Valid from VGG (Note 6)		5.0		5.0		5.0	μs
freq.	Repetition Rate		1.8		1.6		1.0	MHz

CAPACITANCE (Note 7)

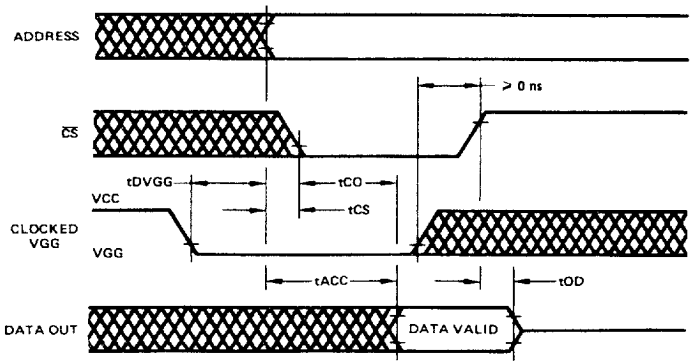
Parameter	Description	Conditions	Typ.	Max.	Unit
CI	Input Capacitance	T_A = 25°C, All unused pins are at VCC	8	15	pF
CO	Output Capacitance		10	15	pF
CVGG	VGG Capacitance			30	pF

SWITCHING WAVEFORMS

READ OPERATION (Note 2)



DESELECTION



CLOCKED VGG OPERATION (Note 1)

The VGG input may be clocked between +5V (VCC) and −9V to save power. To read the data, the chip select ($\overline{CS}$) must be low (≤ VIL) and the VGG level must be lowered to −9V at least tDVGG prior to the address selection. Once the data has appeared at the output and the access time has elapsed, VGG may be raised to +5V. The data output will remain stable for tOHC. To deselect the chip, $\overline{CS}$ is raised to ≥ VIH, and the output will go the high impedance state after tOD. The chip will be deselected when $\overline{CS}$ is raised to VIH whether the VGG is at +5V or at −9V.

PROGRAMMING THE Am1702A

Each storage node in the Am1702A consists of an MOS transistor whose gate is not connected to any circuit element. The transistors are all normally off, making all outputs LOW in an unprogrammed device. A bit is programmed to a HIGH by applying a large negative voltage to the MOS transistor; electrons tunnel through the gate insulation onto the gate itself. When the programming voltage is removed, a charge is left on the gate which holds the transistor on. Since the gate is completely isolated, there is no path by which the charge can escape, except for random high energy electrons which might retunnel through the gate insulation. Under ordinary conditions retunneling is not significant. The application of high energy to the chip through X-rays or UV light (via the quartz window) raises energy levels so that the charge can escape from the gate region, erasing the program and restoring the device to all LOW.

In order to program a specified byte, all 8 address lines must be in the binary complement of the address desired when pulsed VDD and VGG move to their negative level. The complemented address must be stable for at least tACW before VDD and VGG make their negative transitions. The voltage swing of the address lines during programming is between −47V ± 1V and 0V. The addresses must then make a transition to the true state at least tATW before the program pulse is applied. For good data retention, the addresses should be programmed in sequence from 0 to 255, a minimum of 32 times. DO1 through DO8 are used as the data inputs to program the desired pattern. A low level at the data input (−47V ± 1V) will program the selected bit to 1 and a high level (0V) will program it to a 0. All 8 bits addressed are programmed simultaneously.

Programming Boards are available for the Data I/O automatic programmer (part number 1010/1011), for the Spectrum Dynamics programmer (part number 434-549), and for the Pro-Log programmer (part number PM9001).

ERASING THE Am1702A

The Am1702A may be erased (restored to all LOW's) by exposing the die to ultraviolet light from a high intensity source. The recommended dosage is 6 W-sec/cm^2 at a wavelength of 2537 Å. The Ultraviolet Products, Inc., models UVS-54 or S-52 can erase the Am1702A in about 15 minutes, with the devices held one inch from the lamp. (Caution should be used when Am1702A's are inspected under fluorescent lamps after being programmed, as some fluorescent lamps may emit sufficient UV to erase or "soften" the PROM.)

CAUTION

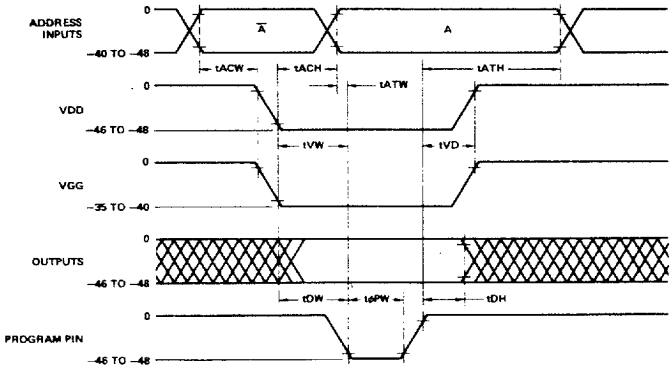
Ultraviolet radiation is invisible and can damage human eyes. Precautions should be taken to avoid exposure to direct or reflected ultraviolet radiation. It will often be convenient to fully enclose the ultraviolet source and the EROMs being erased to prevent accidental exposure.

Ultraviolet lamps can also ionize oxygen and create ozone which is harmful to humans. Erasing should be carried out in a well ventilated area in order to minimize the concentration of ozone.

PROGRAMMING REQUIREMENTS (Note 2)

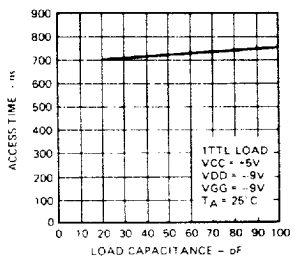
Parameter	Description	Condition	Min.	Typ.	Max.	Unit
ILI1P	Input Current, Address and Data	VI = −48V			10	mA
ILI2P	Input Current, Program and VGG Inputs	VI = −48V			10	mA
IBB	VBB Current			0.05		mA
IDDP	IDD Current During Programming Pulse	VDD = VProg = −48V, VGG = −35V		200	Note 8	mA
VIHP	Input HIGH Voltage				0.3	Volts
VIL1P	Voltage Applied to Output to Program a HIGH		−46		−48	Volts
VIL2P	Input LOW Level on Address Inputs		−40		−48	Volts
VIL3P	Voltage Applied to VDD and Program Inputs		−46		−48	Volts
VIL4P	Voltage Applied to VGG Input		−35		−40	Volts
tφPW	Programming Pulse Width	VGG = −35V, VDD = VProg = −48V			3.0	ms
tDW	Data Set-up Time		25			μs
tDH	Data Hold Time		10			μs
tVW	VGG and VDD Set-up Time		100			μs
tVD	VGG and VDD Hold Time		10		100	μs
tACW	Address Set-up Time (Complement)		25			μs
tACH	Address Hold Time (Complement)		25			μs
tATW	Address Set-up Time (True)		10			μs
tATH	Address Hold Time (True)		10			μs
	Duty Cycle				20	%

PROGRAMMING WAVEFORMS

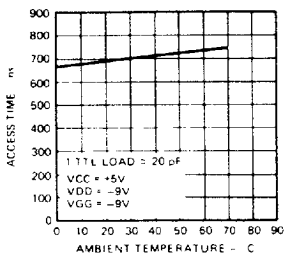


TYPICAL PERFORMANCE CURVES

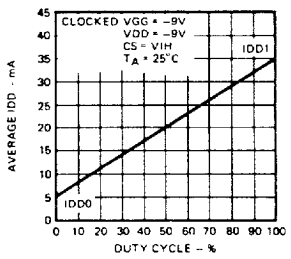
Access Time Versus Load Capacitance



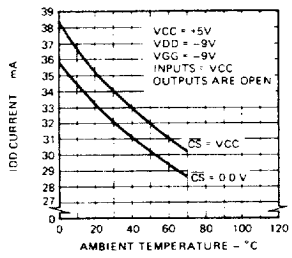
Access Time Versus Temperature



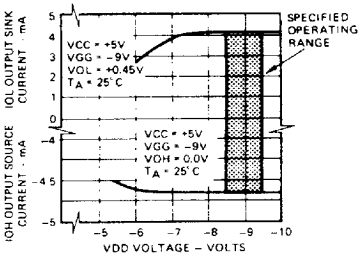
Average Current Versus Duty Cycle for Clocked VGG



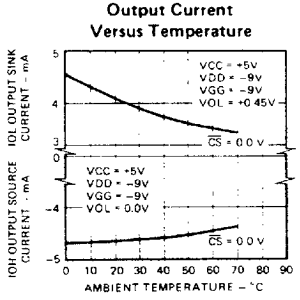
IDD Current Versus Temperature



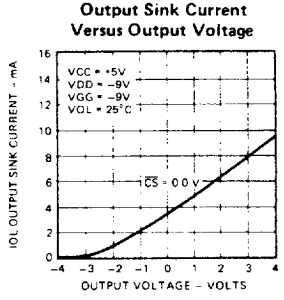
Output Current Versus VDD Supply Voltage



Output Current Versus Temperature



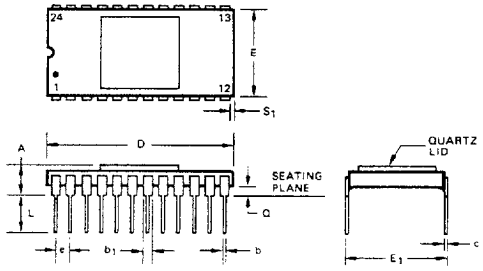
Output Sink Current Versus Output Voltage



NOTES:

1. During read operations VGG may be clocked high to reduce power consumption. This involves swinging VGG up to VCC. See "Clocked VGG Operation". This mode is possible only with the Am1702AL.
2. During Read operations:
   Pins 12, 13, 15, 22, 23 = +5.0V ±5%
   Pins 16, 24 = −9.0V ±5%
   During Program operations:
   T_A = 25°C
   Pins 12, 22, 23 = 0V
   Pins 13, 24 are pulsed low from 0V to −47V ±1V
   Pin 15 = +12.0V ±10%
   Pin 16 is pulsed low from 0V to −37.5V ±2.5V
3. Typical values are for T_A = 25°C, nominal supply voltages and nominal processing parameters.
4. IDD may be reduced by pulsing the VGG supply between VCC and −9V. VDD current will be directly proportional to the VGG duty cycle. The data outputs will be unaffected by address or chip select changes while VGG is at VCC. For this option specify AM1702AL.
5. VIL = 0V, VIH = 4.0V, tr = tf ≤ 50ns, Load = 1 TTL gate.
6. The output will remain valid for tOHC after the VGG pin is raised to VCC, even if address change occurs.
7. These parameters are guaranteed by design and are not 100% tested.
8. Do not allow IDD to exceed 300mA for more than 100μsec.

PHYSICAL DIMENSIONS
24 Pin Side Brazed
Quartz Lid



Reference Symbol	Inches	
	Min.	Max.
A	.100	.200
b	.015	.022
b_1	.030	.060
c	.008	.013
D	1.170	1.200
E	.550	.610
E_1	.590	.620
e	.090	.110
L	.120	.160
Q	.020	.060
S_1	.005	

Note: Dimensions E and D allow for off-center lid, meniscus and glass overrun.