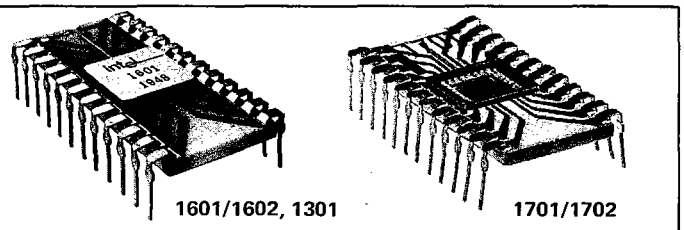
INTEL CORP. 3065 Bowers Avenue, Santa Clara, California 95051 • (408) 246-7501

1601/1701,1602/1702 ELECTRICALLY PROGRAMMABLE 1301 MASK PROGRAMMABLE

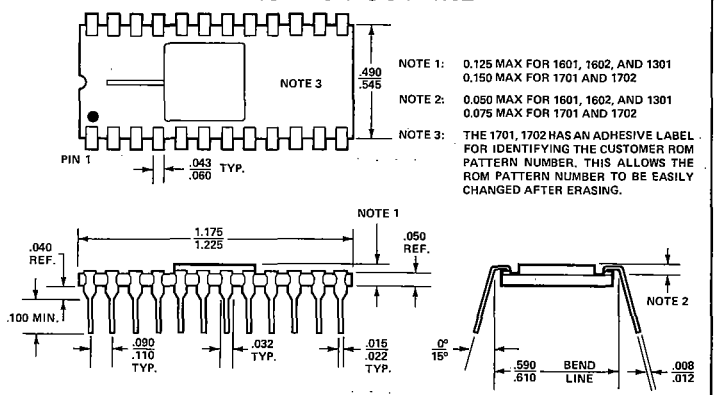
2048 BIT FULLY DECODED READ ONLY MEMORY

SEPTEMBER 1971

- Erasable and Field Reprogrammable (1701,1702)
- Field Programmable (1601,1602)
- All 2048 Bits Guaranteed Programmable – 100% factory tested (1601/1701,1602/1702)
- Inputs and outputs DTL and TTL compatible
- Static and Dynamic Operation (1601,1701,1301)
- Static Only Operation (1602,1702)
- OR-tie capability
- Simple Memory Expansion – Chip Select input lead
- 24 pin dual-in-line hermetically sealed ceramic package (1601,1602,1301)
- 24 pin dual-in-line, quartz lid ceramic package (1701,1702)



PACKAGE OUTLINE

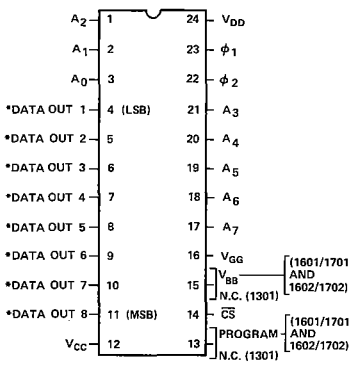


NOTE 1: 0.125 MAX FOR 1601, 1602, AND 1301
0.150 MAX FOR 1701 AND 1702

NOTE 2: 0.050 MAX FOR 1601, 1602, AND 1301
0.075 MAX FOR 1701 AND 1702

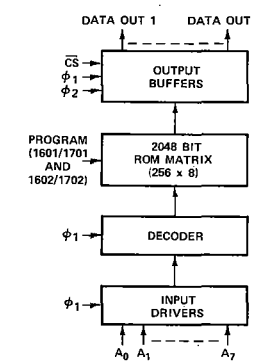
NOTE 3: THE 1701, 1702 HAS AN ADHESIVE LABEL FOR IDENTIFYING THE CUSTOMER ROM PATTERN NUMBER. THIS ALLOWS THE ROM PATTERN NUMBER TO BE EASILY CHANGED AFTER ERASING.

PIN CONFIGURATION



*THIS PIN IS THE DATA INPUT LEAD FOR THE 1601/1701 AND 1602/1702 DURING PROGRAMMING

BLOCK DIAGRAM



NOTE: LOGIC 1 AT INPUT AND OUTPUT IS A HIGH AND LOGIC 0 IS LOW.

The Intel 1601, 1602, 1701, and 1702 is a 256 word by 8 bit electrically programmable ROM ideally suited for uses where fast turnaround and pattern experimentation are important such as in prototype or in one of a kind systems. The 1601, 1602, 1701, and 1702 is factory reprogrammable which allows Intel to perform a complete programming and functional test on each bit position before delivery.

The four devices 1601, 1602, 1701, and 1702 use identical chips. The 1601 and 1701 is operable in both the static and dynamie mode while the 1602 and 1702 is operable in the static mode only. Also, the 1701 and 1702 has the unique feature of being completely erasable and field reprogrammable. This is accomplished by a quartz lid that allows high intensity ultraviolet light to erase the 1701 and 1702. A new pattern can then be written into the device. This procedure can be repeated as many times as required.

The 1301 is a direct replacement part which is programmed by a metal mask and is ideal for large volume and lower cost production runs of systems initially using the 1601/1701 or the static only 1602/1702.

The dynamic mode of the 1601/1701 and 1301 refers to the decoding circuitry and not to the memory cell. Dynamic operation offers higher speed and lower power dissipation than the static operation.

The 1601, 1602, 1701, and 1702 is fabricated with silicon gate technology. This low threshold technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

STATIC, DYNAMIC, PROGRAMMING MODE PIN CONNECTIONS

To operate the 1601/1701, 1602/1702, 1301 in either a static, dynamic, or programming (1601/1701, 1602/1702) mode[1], the following external lead connections are required in addition to those shown by the pin configuration diagram on page 1.

PIN / MODE	13[2] (Program)	15[2] (V_{BB})	16 (V_{GG})	22 (ϕ_2)	23 (ϕ_1)
Static	V_{CC}	V_{CC}	V_{GG}	V_{CC}	V_{CC}
Dynamic (1601/1701, 1301)	$\emptyset_1$	V_{CC}	V_{CC}	$\emptyset_2$	$\emptyset_1$
Programming (1601/1701,1602/1702)	Program Pulse	V_{BB}	Pulsed V_{GG} (V_{IL4P})	GND	GND

Absolute Maximum Ratings*

Case Temperature Under Bias	0°C to +85°C
Storage 1601/1701, 1602/1702	−65°C to +125°C
Temperature: 1301	−65°C to +160°C
Soldering Temperature of Leads (10 sec)	+300°C
Power Dissipation	1 Watt
Static and Dynamic Operation: Input Voltages and Supply Voltages with respect to V_{CC}	+0.5V to −20V
Program Operation: Input Voltages and Supply Voltages with respect to V_{CC}	−50V

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

STATIC OPERATION FOR 1601/1701, 1602/1702 AND 1301

D.C. and Operating Characteristics for Static Operation

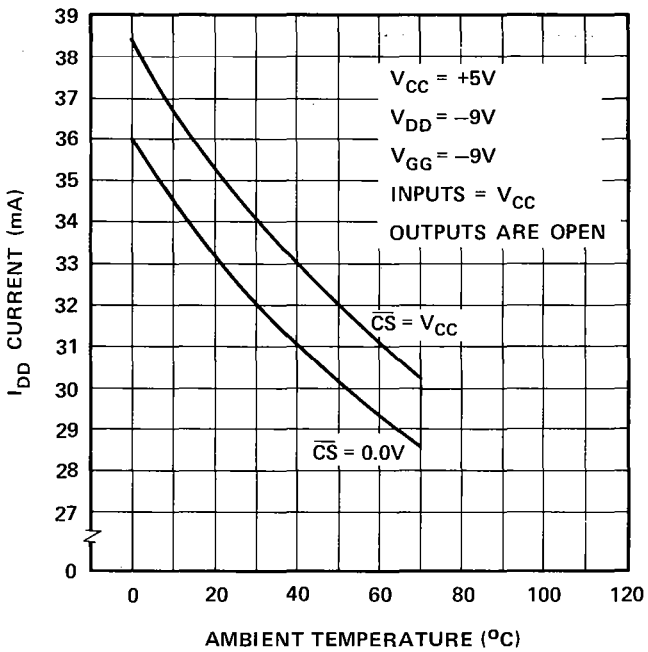
T_A = 0°C to 70°C, V_{CC} = +5V±5%, V_{DD} = −9V±5%, V_{GG}[3] = −9V±5%, unless otherwise noted.

SYMBOL	TEST	MIN.	TYP.[4]	MAX.	UNIT	CONDITIONS
I_{LI}	Address and Chip Select Input Load Current			1	µA	V_{IN} = 0.0V
I_{LO}	Output Leakage Current			1	µA	V_{OUT} = 0.0V, $\overline{CS}$ = V_{CC} −2
I_{DDO}	Power Supply Current		5	10	mA	V_{GG}=V_{CC}, $\overline{CS}$=V_{CC}−2 I_{OL}= 0.0mA, T_A = 25°C
I_{DD1}[5]	Power Supply Current		35	50	mA	$\overline{CS}$=V_{CC} −2 I_{OL} =0.0mA, T_A = 25°C
I_{DD2}[5]	Power Supply Current		32	46	mA	$\overline{CS}$=0.0 I_{OL} =0.0mA, T_A = 25°C
I_{DD3}[5]	Power Supply Current		38.5	60	mA	$\overline{CS}$=V_{CC} −2 I_{OL} =0.0mA , T_A = 0°C
I_{GG}	Gate Supply Current			1	µA	
V_{IL}	Address and Chip Select Input Low Voltage	V_{CC}−10		V_{CC}−4.2	V	
V_{IH}	Address and Chip Select Input High Voltage	V_{CC}−2		V_{CC}+.3	V	
I_{OL}	Output Sink Current	1.6	4		mA	V_{OUT} = 0.45V
I_{CF}	Output Clamp Current		8	13	mA	V_{OUT} = −1.0V
I_{OH}	Output Source Current	−2.0			mA	V_{OUT} = 0.0V
V_{OL}	Output Low Voltage		−.7	0.45	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage	3.5	4.5		V	I_{OH} = −100 µA

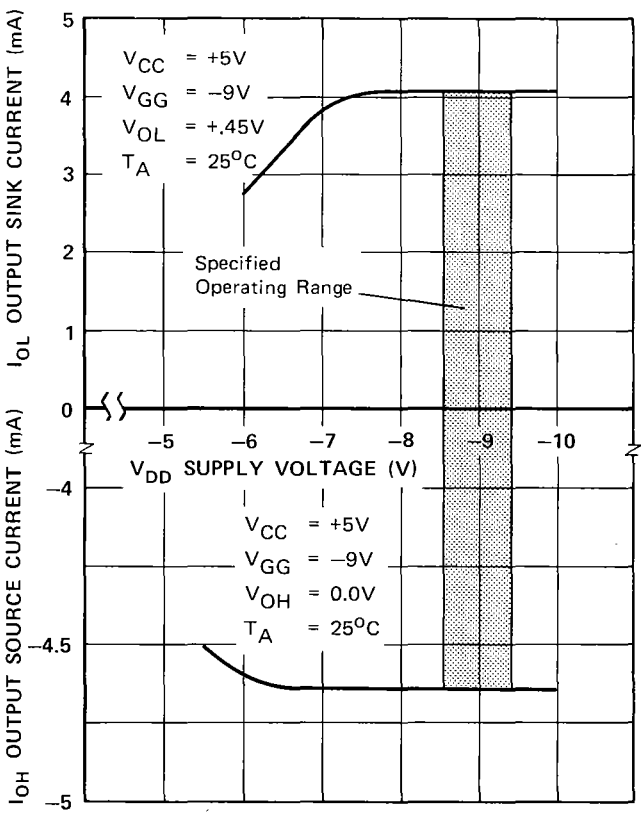
Note 1: In the programming mode, the data inputs 1–8 are pins 4–11 respectively. $\overline{CS}$ = GND.
Note 2: This external lead connection is only necessary on the 1601/1701 and 1602/1702. It may be unconnected on the 1301.
Note 3: V_{GG} may be clocked to reduce power dissipation. In this mode average I_{DD} increases in proportion to V_{GG} duty cycle. (See p. 5)
Note 4: Typical values are at nominal voltages and T_A = 25°C.
Note 5: Measured under continuous operation.

Typical Characteristics for Static Operation

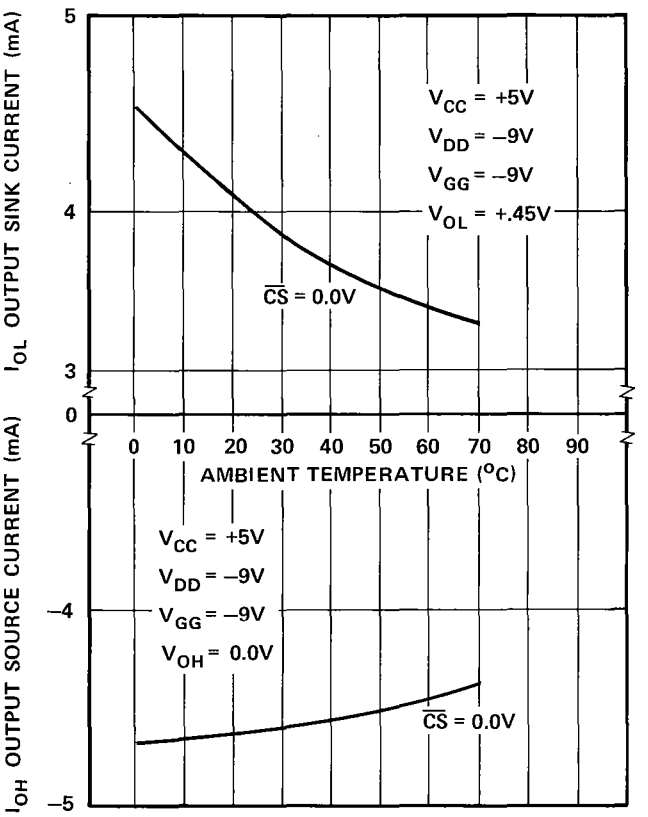
I_{DD} CURRENT VS. TEMPERATURE



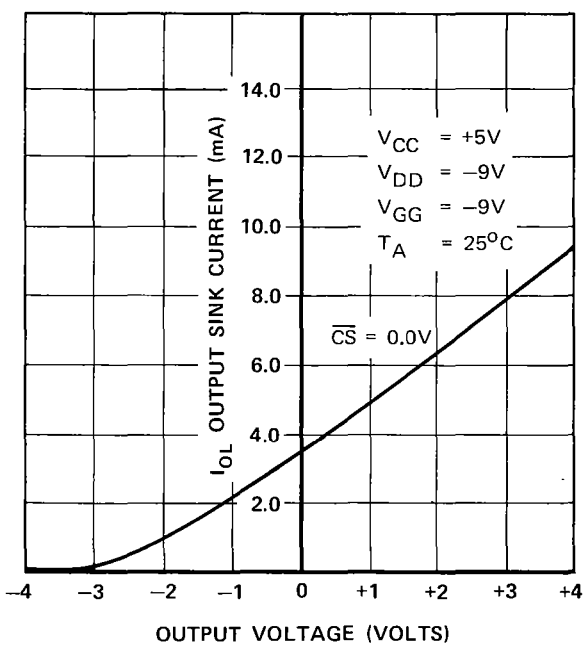
OUTPUT CURRENT VS. V_{DD} SUPPLY VOLTAGE



OUTPUT CURRENT VS. TEMPERATURE



OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



A.C. Characteristics for Static Operation

T_A = 0° C to +70° C, V_{CC} = +5V ±5%, V_{DD} = −9V ±5%, V_{GG} = −9V ±5% unless otherwise noted

SYMBOL	TEST	1601/1701, 1602/1702 MIN.	TYP.	MAX.	1301 MIN.	TYP.	MAX.	UNIT
Freq	Repitition rate			1			1.1	Mhz
t_{OH}	Previous read data valid			100			100	ns
t_{ACC}	Address to output delay		.700	1			.900	μs
t_{DVGG}	Clocked V_{GG} set up	0			1			μs
t_{CS}	Chip select delay			100			200	ns
t_{CO}	Output delay from $\overline{CS}$			900			500	ns
t_{OD}	Output deselect			300			300	ns
t_{OHC}	Data out hold in clocked V_{GG} mode (Note 1)			5			5	μs
C	Capacitance		See page 10			See page 10		

NOTE 1: The output will remain valid for t_{OHC} as long as clocked V_{GG} is at V_{CC}. An address change may occur as soon as the output is sensed (clocked V_{GG} may still be at V_{CC}). Data becomes invalid for the new address when clocked V_{GG} is returned to V_{GG}.

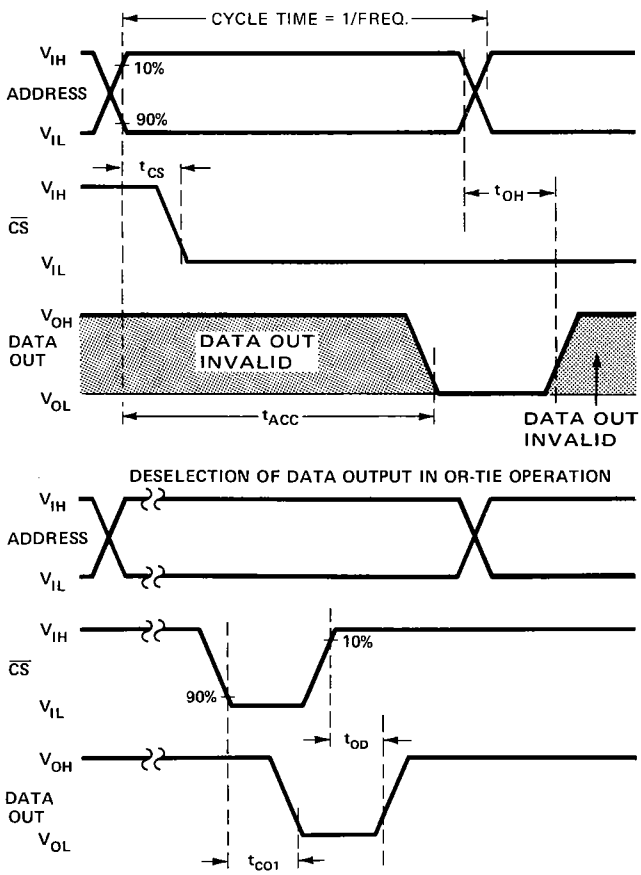
Switching Characteristics for Static Operation

Conditions of Test:

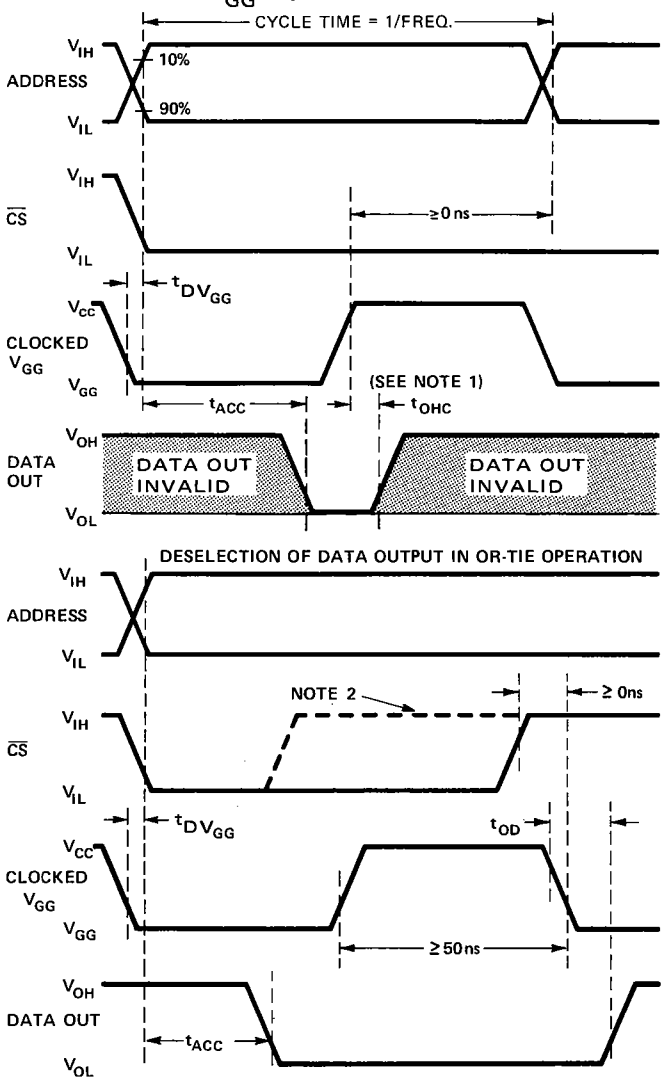
Input pulse amplitudes: 0 to 4V; t_R, t_F ≤50 ns

Output load is 1 TTL gate; measurements made at output of TTL gate (t_{PD} ≤15 ns)

A) Normal Operation (Constant V_{GG})



B) Clocked V_{GG} Operation

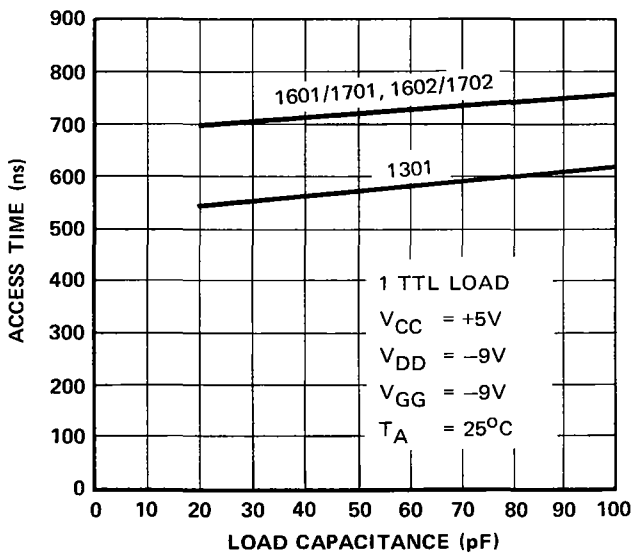


NOTE 1: The output will remain valid for t_{OHC} as long as clocked V_{GG} is at V_{CC}. An address change may occur as soon as the output is sensed (clocked V_{GG} may still be at V_{CC}). Data becomes invalid for the new address when clocked V_{GG} is returned to V_{GG}.

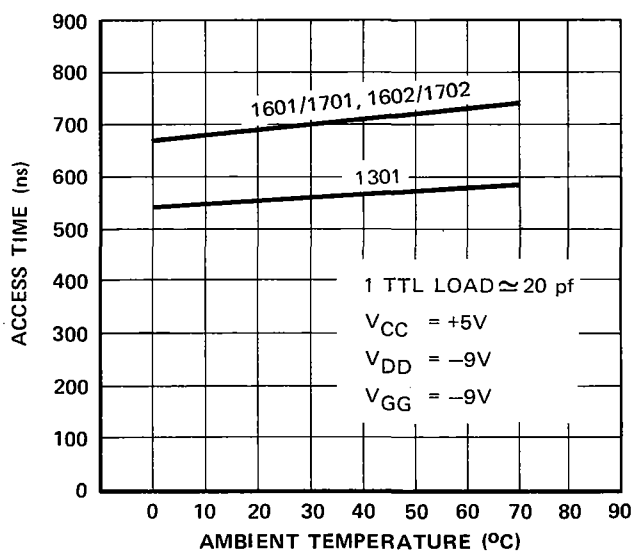
NOTE 2: If $\overline{CS}$ makes a transition from V_{IL} to V_{IH} while clocked V_{GG} is at V_{GG}, then deselection of output occurs at t_{OD} as shown in static operation with constant V_{GG}.

Typical Characteristics for Static Operation

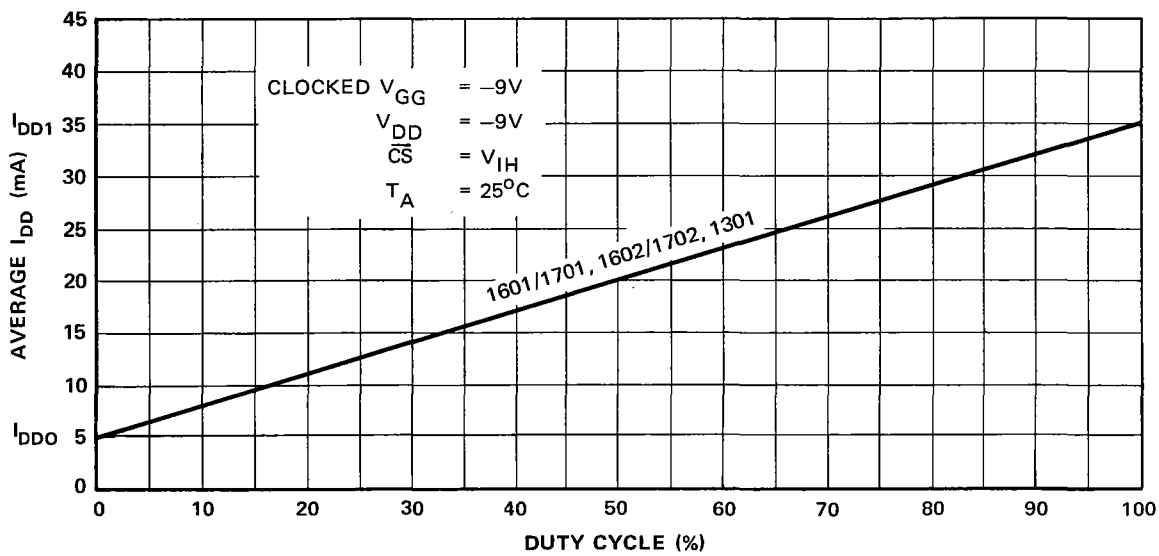
ACCESS TIME VS. LOAD CAPACITANCE



ACCESS TIME VS. TEMPERATURE



AVERAGE CURRENT VS. DUTY CYCLE FOR CLOCKED V_{GG}



DYNAMIC OPERATION FOR 1601/1701 AND 1301 ONLY

D.C. and Operating Characteristics for Dynamic Operation

T_A = 0°C to +70°C, V_{CC} = V_{GG} = +5V ±5%, V_{DD} = −9V ±5%, unless otherwise noted

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_{LI}	Address and Chip Select Input Load Current			1	µA	V_{IN} = 0.0V
I_{LC}	Ø1, Ø2 Clock Leakage Current			10	µA	V_{ILC} = V_{CC} −14.5
I_{LO}	Output Leakage Current			10	µA	V_{out} = 0.0V $\overline{CS}$ = V_{CC} −2
I_{DDO}	Average Power Supply Current		5	10	mA	Clock Voltages = V_{IHC} T_A = 25°C, $\overline{CS}$ = V_{CC} −2
*I_{DD4}	Average Power 1601/1701		30	45	mA	$\overline{CS}$ = V_{CC} −2 1 Mhz rate; clock width at min spec value
	Supply Current 1301		28	40	mA	
	@ T_A = 25°C					
*I_{DD5}	Average Power 1601/1701			55	mA	
	Supply Current 1301			50	mA	
	@ T_{case} = 0°C					
V_{IL}	Address and Chip Select Input Low Voltage	V_{CC} −10		V_{CC} −4.2	V	
V_{ILC}	Ø1, Ø2 Input Low Voltage	V_{CC} −14.5		V_{CC} −12.6	V	
V_{IH}	Address and Chip Select Input High Voltage	V_{CC} −2		V_{CC} +.3	V	
V_{IHC}	Ø1, Ø2 Input High Voltage	V_{CC} −1		V_{CC} +.3	V	
I_{OL}	Output Sink Current	1.6			mA	V_{out} = 0.45V
I_{CF}	Output Clamp Current		8	13	mA	V_{out} = −1.0V
I_{OH}	Output Source Current	−2			mA	V_{out} = 0.0V
V_{OL}	Output Low Voltage		−.7	0.45	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage	3.5	4.5		V	I_{OH} = −100µA

*I_{DD} flows mainly during $t_{\phi 1PW}$. I_{DD} is directly proportional to ϕ_1 clock duty cycle.

A.C. Characteristics for Dynamic Operation

T_A = 0°C to +70°C, V_{CC} = +5V ±5%, V_{DD} = −9V ±5% unless otherwise noted

SYMBOL	TEST	1601, 1701			1301			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
$t_{\phi 1PW}$	ϕ_1 Clock Pulse Width	0.260		2	0.260		2	μs
$t_{\phi 2PW}$	ϕ_2 Clock Pulse Width	0.140		2	0.140		2	μs
$t_{\phi D1}$	ϕ_2 delay from ϕ_1	0.150		2	0.150		2	μs
$t_{\phi D2}$	ϕ_1 delay from ϕ_2	0.05			0.05			μs
t_r, t_f	Clock Pulse Transition			50			50	ns
t_{ACC1}	Address to Output Access		450	650		450	650	ns
t_{ACC2}	Output Access from ϕ_2			130			130	ns
t_{CD}	Chip Select to ϕ_1 Overlap	0			0			ns
t_{DES}	Deselection of Data Output			150			150	ns
C	Capacitance	See page 10			See page 10			

Switching Characteristics for Dynamic Operation

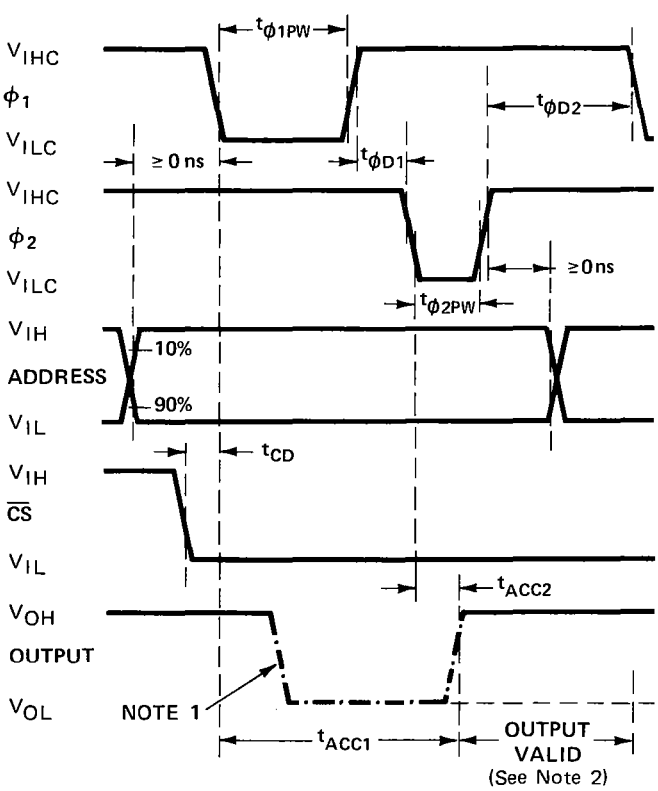
DYNAMIC OPERATION

Conditions of Test:

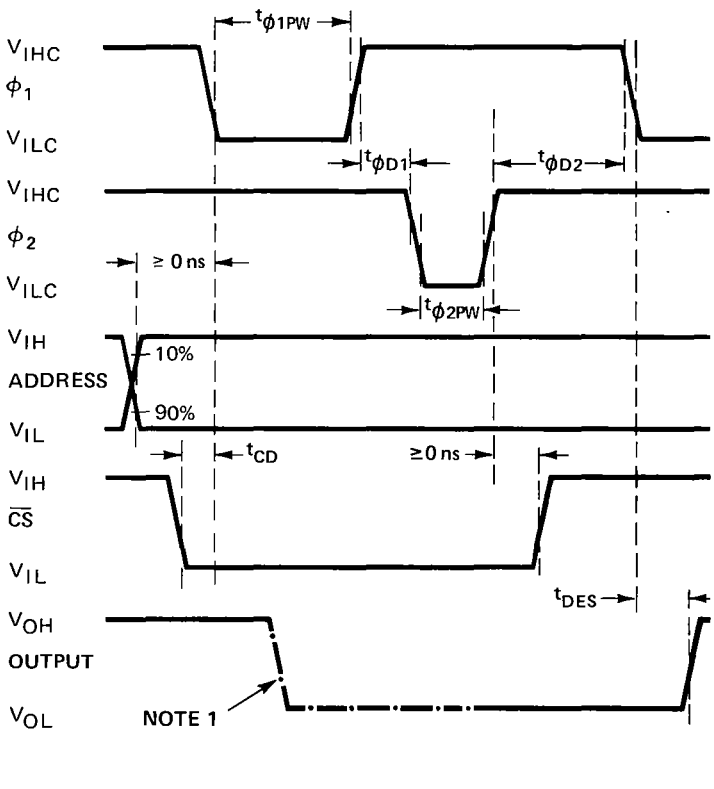
Input pulse amplitudes: 0 to 4V, Input pulse rise and fall times ≤50 nsec

Output load is 1 TTL gate; measurements made at output of TTL gate (t_{pd} ≤ 15 nsec)

A) Normal Operation



B) Deselection of Data Output In OR-tie Operation

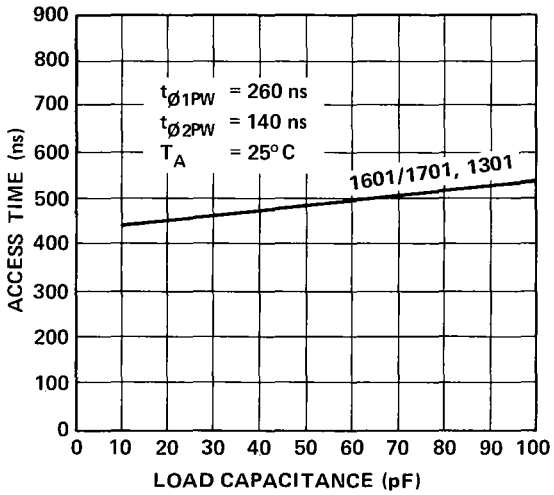


Note 1: An output low transition occurs for every ϕ_1 period independent of memory information.

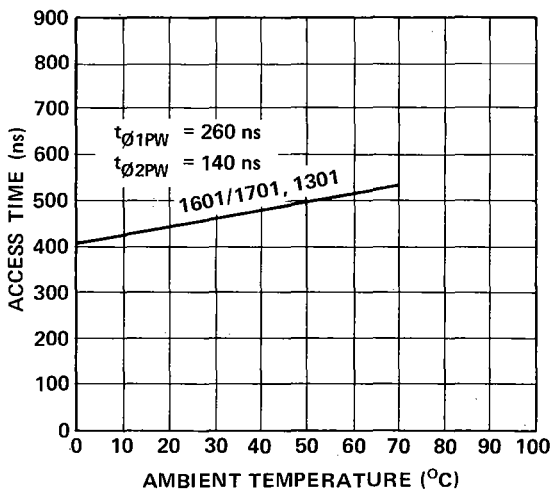
Note 2: Output will remain valid for 2 μsec as long as ϕ_1 does not occur.

Typical Characteristics for Dynamic Operation

ACCESS TIME VS. LOAD CAPACITANCE



ACCESS TIME VS. TEMPERATURE



PROGRAMMING OPERATION FOR THE 1601/1701 AND 1602/1702 ONLY

D.C. and Operating Characteristics for Programming Operation

$T_A = 25°C$, $V_{CC} = 0V$, $V_{BB} = +12V \pm 10\%$, $\overline{CS} = 0V$ unless otherwise noted

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_{LI1P}	Address and Data Input Load Current	10			mA	$V_{IN} = -40V$
I_{LI2P}	Program and V_{GG} Load Current	10			mA	$V_{IN} = -48V$
I_{BB}	V_{BB} Supply Load Current		.05	1	mA	
I_{DDP}(1)	Peak I_{DD} Supply Load Current		750		mA	$V_{DD} = V_{prog} = -50V$ $V_{GG} = -35V$
V_{IHP}	Input High Voltage			0.3	V	
V_{IL1P}	Pulsed Data Input Low Voltage	−40		−48	V	
V_{IL2P}	Address Input Low Voltage	−40		−48	V	
V_{IL3P}	Pulsed Input Low V_{DD} and Program Voltage	−48		−50	V	
V_{IL4P}	Pulsed Input Low V_{GG} Voltage	−35		−40	V	

Note 1: I_{DDP} flows only during program period $t_{\phi PW}$.
Average power supply current I_{DDP} is typically 15 mA at 2% duty cycle.

A.C. Characteristics for Programming Operation

($T_{AMBIENT}$ = 25°C, V_{CC} = 0V, V_{BB} = + 12V ± 10%, $\overline{CS}$ = 0V unless otherwise noted

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
	Duty Cycle			2	%	
$t_{\phi PW}$(1)	Program Pulse Width			20	ms	V_{GG}=−35V,V_{DD}=$V_{program}$=−48V
t_{DW}	Data Set Up Time	1			µs	
t_{DH}	Data Hold Time	1			µs	
t_{VD}	Pulsed V_{GG} and V_{DD} Supply Overlap	1			µs	
C	Capacitance	See page 10				

Note 1: Maximum duty cycle of $t_{\phi PW}$ should not be greater than 2% of cycle time so that power dissipation is minimized. To guarantee long term memory retention the program cycle should be repeated five times with $t_{\phi PW}$ = 20 msec or the equivalent thereof, e.g. 10 cycles of $t_{\phi PW}$ = 10 msec.

Switching Characteristics for Programming Operation

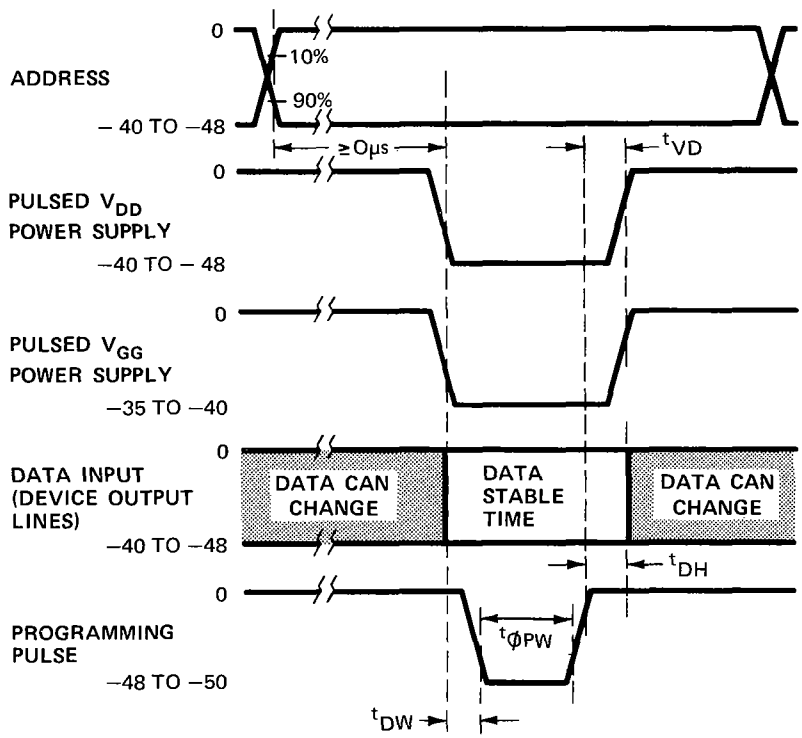
PROGRAM OPERATION

Conditions of Test:

Input pulse rise and fall times ≤250nsec

$\overline{CS}$ = 0V

PROGRAM WAVEFORMS



Programming Operation of the 1601/1701 and 1602/1702

When the Data Input for the Program Mode is:	Then the Data Output during the Read Mode is:
$V_{IL1P} = \sim -40V$ pulsed	Logic 1 = V_{OH} = 'P' on tape
$V_{IHP} = \sim 0V$	Logic 0 = V_{OL} = 'N' on tape

WORD \ ADDRESS	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
|	|	|	|	|	|	|	|	|
|	|	|	|	|	|	|	|	|
255	1	1	1	1	1	1	1	1

Address Logic Level During Read Mode: Logic 0 = V_{IL} ($\sim$.3V) Logic 1 = V_{IH} ($\sim$3V)

Address Logic Level During Program Mode:* Logic 0 = V_{IL2P} ($\sim -40V$) Logic 1 = V_{IHP} ($\sim$0V)

*The Logic Levels for the address inputs are inverted from the Logic Levels for the data inputs during the Program Mode.

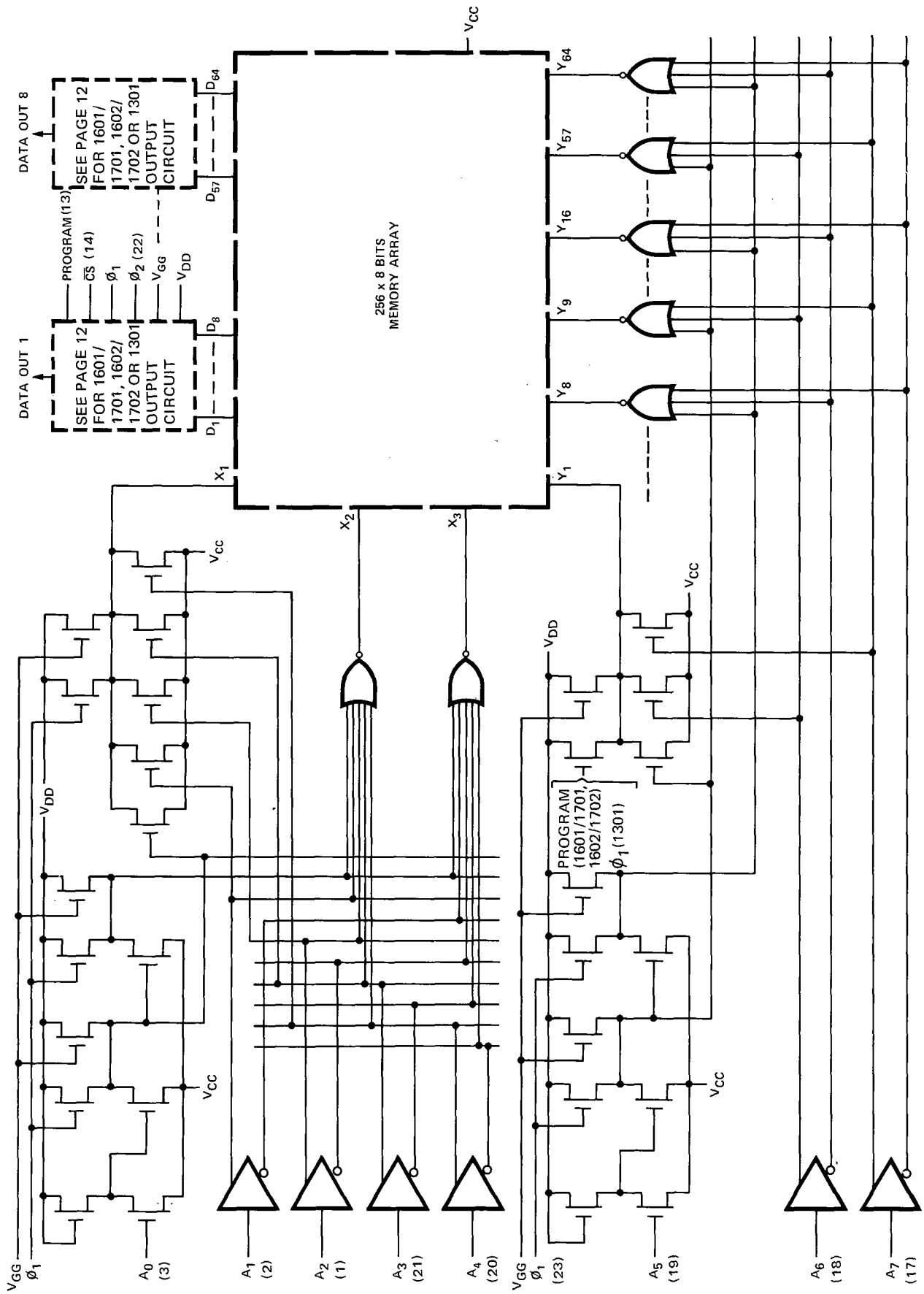
CAPACITANCE*
A.C. Characteristics, T_A = 25°C

SYMBOL	TEST	1601/1701, 1602/1702 MIN.	TYP.	MAX.	1301 MIN.	TYP.	MAX.	UNIT	CONDITIONS
C_{IN}	Input Capacitance		8	15		5	10	pF	$V_{IN}=V_{CC}$, $\overline{CS}=V_{CC}$
C_{out}	Output Capacitance		10	15		5	10	pF	$V_{out}=V_{CC}$, $\overline{CS}=V_{CC}$
$C_{\phi 1}$	ϕ_1 Clock Capacitance (includes pin 13)		35	55		20	30	pF	$V_{\phi 1}=V_{CC}$
$C_{\phi 2}$	ϕ_2 Clock Capacitance		9	15		7	15	pF	$V_{\phi 2}=V_{CC}$
$C_{V_{GG}}$	V_{GG} Capacitance (Clocked V_{GG} Mode)			30			30	pF	$V_{GG}=V_{CC}$

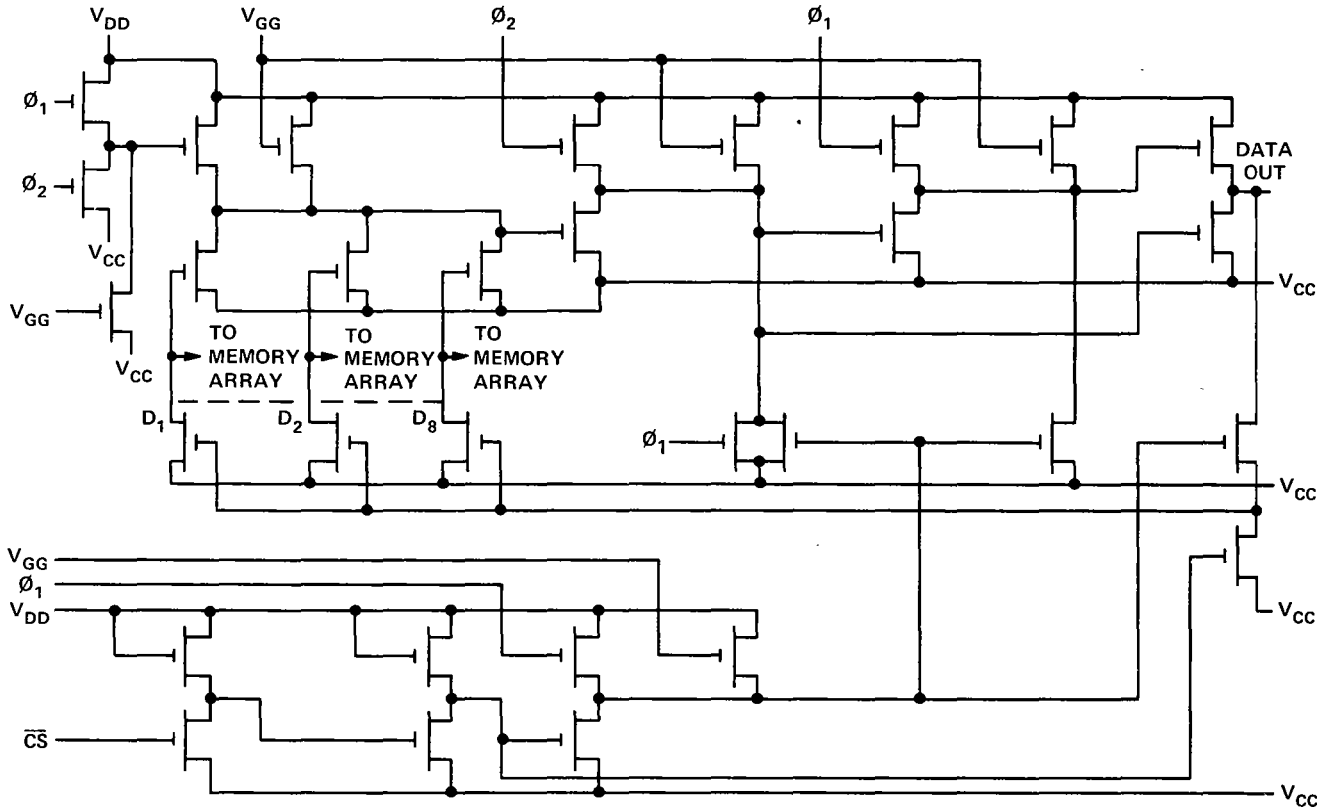
All unused pins are at A.C. ground

*This parameter is periodically sampled and is not 100% tested

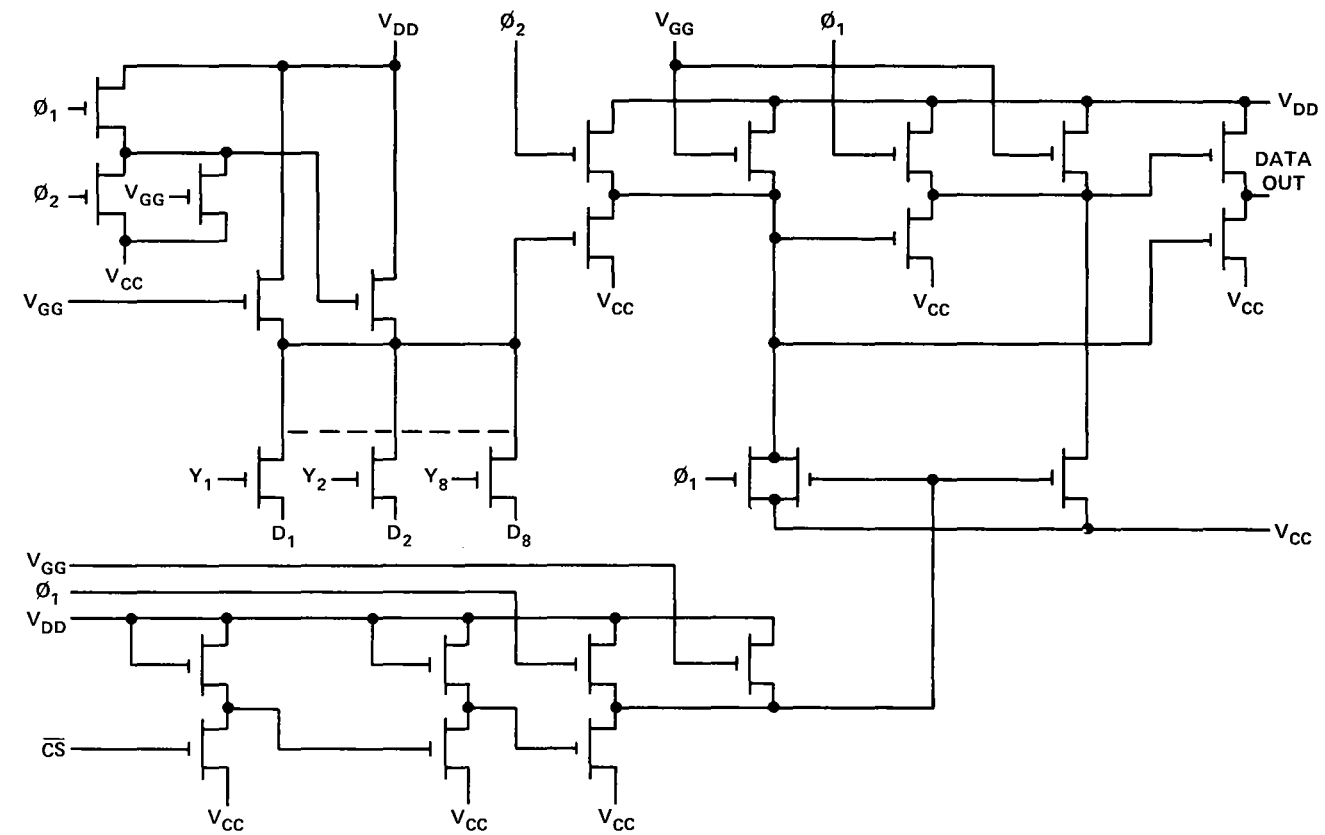
1601/1701, 1602/1702, 1301 Circuit Schematic



1 of 8 Output Circuits 1601/1701, 1602/1702



1 of 8 Output Circuits 1301



Application Information

I. OPERATION OF THE 1601/1701 AND 1602/1702 IN PROGRAM MODE

Initially, all 2048 bits of the ROM are in the "1" state (output high). Information is introduced by selectively programming "0"s (output low) in the proper bit locations.

Word address selection is done by the same decoding circuitry used in the READ mode (see table on page 10 for logic levels). The eight output terminals are used as data inputs to determine the information pattern in the eight bits of each word. A low data input level (−40V) will leave a "1" and a high data input level (ground) will allow programming of "0" (see table on page 10). All eight bits of one word are programmed simultaneously by setting the desired bit information patterns on the data input terminals. The duty cycle of the Program pulse (amplitude and width as specified on page 10) should be limited to 2%. The address should be applied for at lease 1 μsec before application of the Program pulse.

During the programming, V_{GG}, V_{DD} and the Program Pulse are pulsed signals.

II. MANUAL PROGRAMMING OF THE 1601, 1602, 1701, AND 1702

The 1601, 1602, 1701, or 1702, may be programmed by a machine such as the 7600 programmer or manually using a circuit similar to the one on pages 14 and 15. A parts list (pages 16 and 17) and the circuit board layout (pages 16 and 17) is also given. The circuit is capable of programming as well as reading the ROM. Programming takes approximately one hour.

Circuit Operation

1. In the read mode, the 1601, 1602, 1701, or 1702, is operated with V_{CC}=0 and V_{DD} =−14V (rather than +5 and −9V). The ROM is biased for static operation, and the sensed output signals from the ROM are used to drive transistors which in turn drive LED display devices. Input addresses are biased at levels of 0V and −5V for logic 1 and logic 0 respectively.

2. In the write mode, the 1601, 1602, 1701, or 1702, is operated in a pulsed mode. An astable multivibrator, running at about 2 pulses per second, drives a transistor which normally biases the negative regulator off. At each pulse, the negative regulator is allowed to apply −48 to −50 volts to the V_{DD} terminal of the ROM. Address and data voltages are derived using a simple emitter follower circuit as a regulator. V_{GG} during programming is derived using a zener diode and a resistive divider. In read mode, this circuit causes V_{GG} to equal V_{DD}. During each V_{DD} pulse, the program pulse is held off for about 2 μsec using a 100 pF capacitor, 47K resistor and 1N914 diode at the input of the program pulse driver circuit. The program pulse driver is biased to turn off prior to turn off of the V_{DD} pulse.

The entire circuit can be operated from a single −60V to −80V unregulated source. The +12V V_{BB} needed during programming is derived using a capacitive coupled circuit with a 12V zener regulator.

Program pulses average about 10 msec in length. At two per second, the circuit must be operated for 5 seconds to achieve a total of 100 msec of program pulses. The rate of 10 msec of program pulse every .5 second insures that a 2% programming duty cycle will not be exceeded.

Circuit Checkout (to be done before plugging in a Unit)

1. Set the read/write, 4PDT switch ($S1_A$ through $S1_D$) to the R(Read) position:
   (a) Adjust the (V_{DD}, RD) resistor so that V_{DD} reads −14 volts (T.P.1)

2. Set the read/write, 4PDT switch to the W(Write) position. Depress the "Write" push button and hold for the following sequence of adjustments. **They must be done in the order shown:**
   (a) Adjust the (V_{DD}, PR) resistor so that V_{DD} reads −49 volts (T.P.1).
   (b) Adjust the (V_{GG}, ADJ) resistor so that V_{GG} reads −36 volts (T.P.2).
   (c) Adjust the (V_{ADR}, ADJ) resistor so that V_{ADR} reads −40 volts (T.P.3).

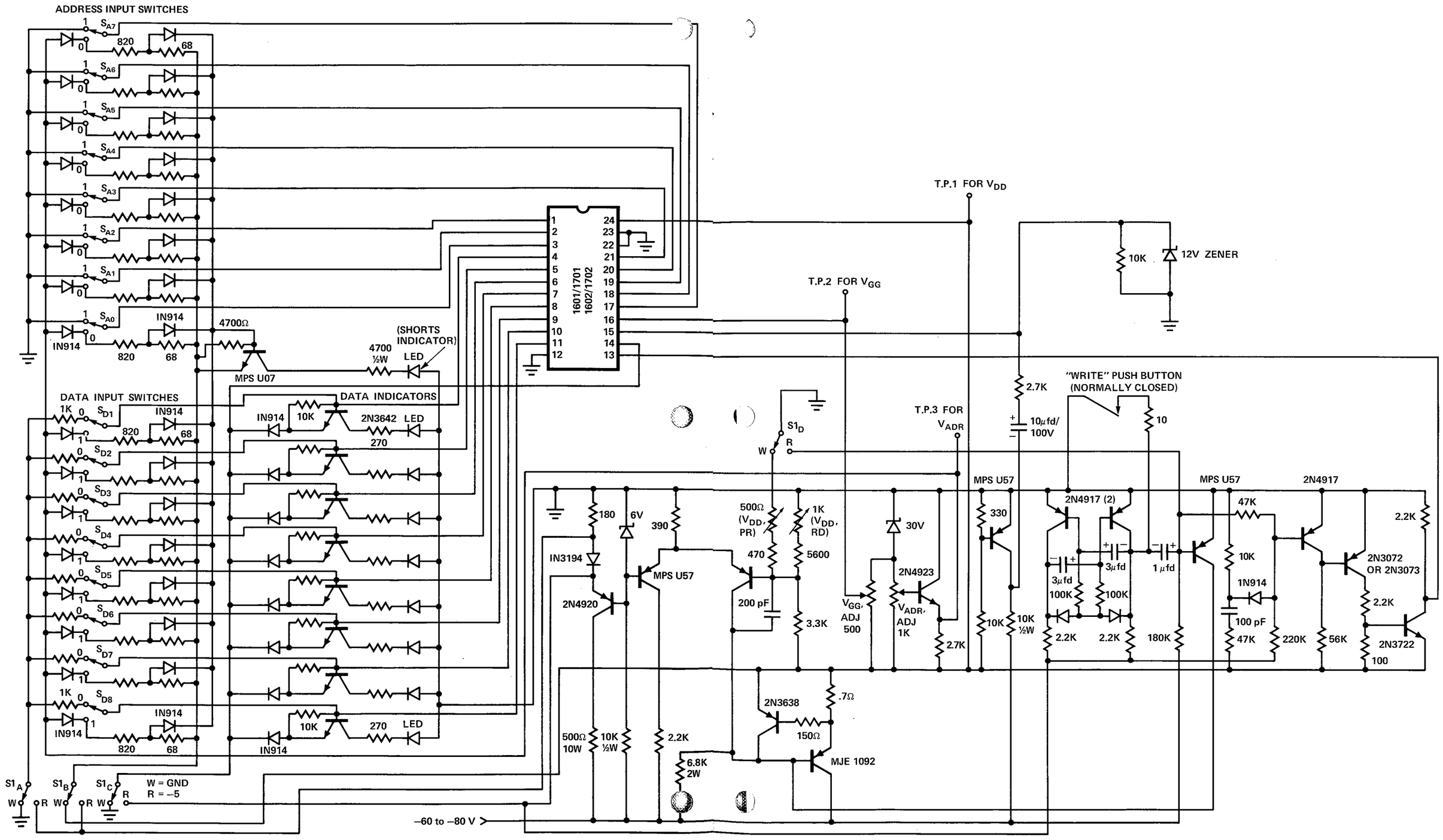
3. While the read/write switch is in the write position, the shorts indicator should be checked to see if there are any shorts on the data or address input pins. This would be indicated by the shorts indicator flashing when the "write" push button is depressed.

See page 18 for Programming Instructions For Manual Programmer

Intel cannot assume responsibility for the programming circuit described in this data sheet.

Circuit Schematic

1601/1701 BASIC MANUAL PROGRAMMER



PARTS LIST

Resistors	Quantity
0.7 Ω½W	1 ea.
10 Ω	1 ea.
68 Ω	16 ea.
100 Ω	2 ea.
270 Ω	8 ea.
330 Ω	1 ea.
390 Ω	1 ea.
680 Ω	1 ea.
820 Ω	16 ea.
1000 Ω	8 ea.
2000 Ω	1 ea.
2200 Ω½W	2 ea.
2200 Ω	3 ea.
2700 Ω	2 ea.
3.3K Ω	1 ea.
4.7K Ω	1 ea.
4.7K Ω½W	1 ea.
6.8K Ω2W	1 ea.
10K Ω	11 Ea.
10K Ω½W	2 ea.
47K Ω	2 ea.
56K Ω	1 ea.
100K Ω	2 ea.
180K Ω	1 ea.
220K Ω	1 ea.
500 Ω10W	1 ea.
500 Ω Trim Pot 1W	2 ea.
1000 ΩTrim Pot 1W	2 ea.

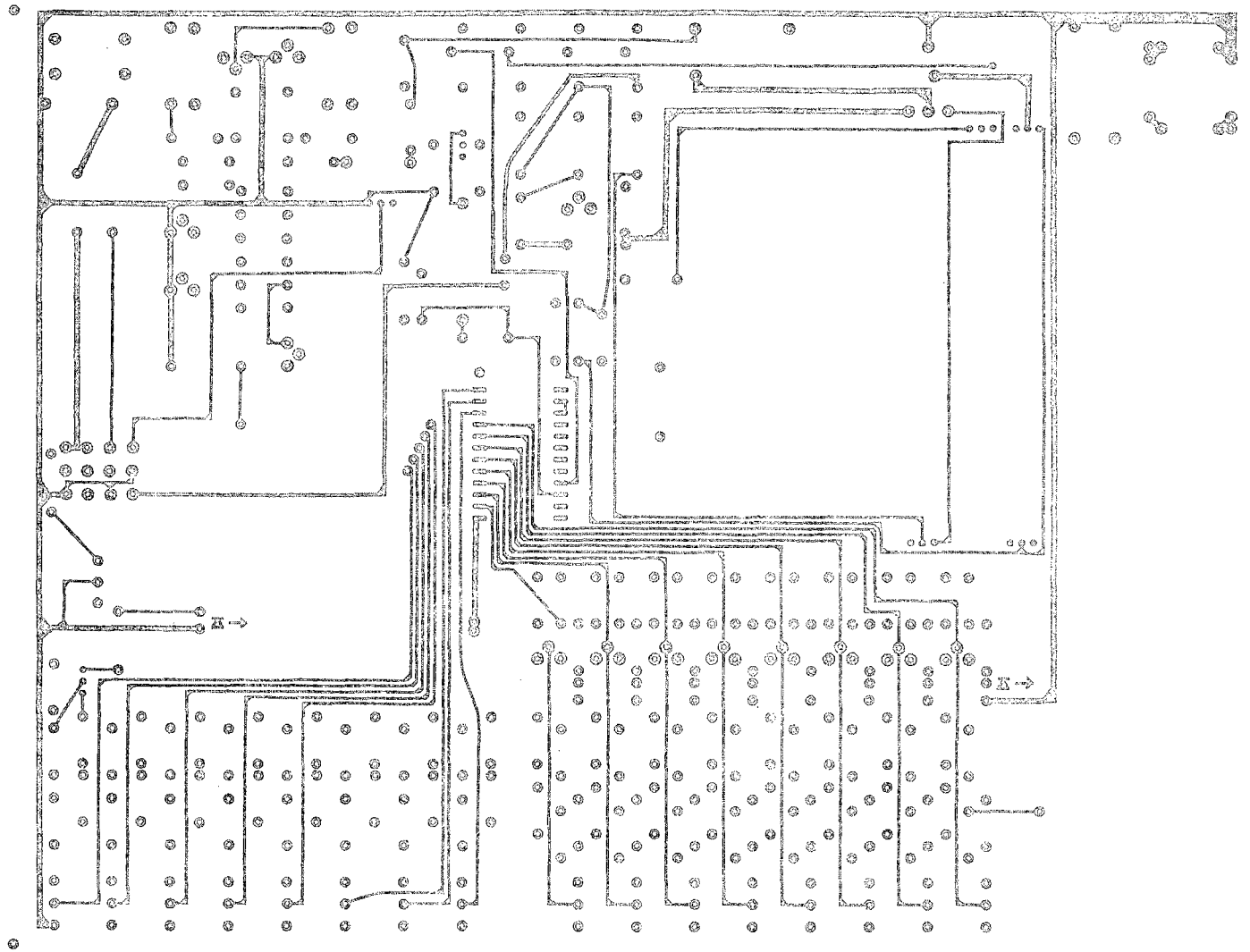
NOTE: All Resistors are 1/4 watt 10% unless marked otherwise

Capacitors	Quantity
10μf 100V	1 ea.
3.3μf 15V	2 ea.
1.0μf 35V	1 ea.
200 pF Mica	1 ea.
100 pF Mica	1 ea.

Semiconductors	Quantity
IN914	43 ea.
IN3194	1 ea.
IN5233 6.0V Zener	1 ea.
IN5242 12.0V Zener	1 ea.
IN5256 30.0V Zener	1 ea.
MJE1092	1 ea.
MPS-U57	4 ea.
MPS-U07	1 ea.
2N4920	1 ea.
2N4923	1 ea.
2N4917	3 ea.
2N3073	1 ea.
2N3722	1 ea.
MV-10B L.E.D.	9 ea.
2N3642	8 ea.
2N3638	1 ea.

Switches	Quantity
SPDT Toggle	16 ea.
4PDT Toggle	1 ea.
SPST Push Button N.C.	1 ea.

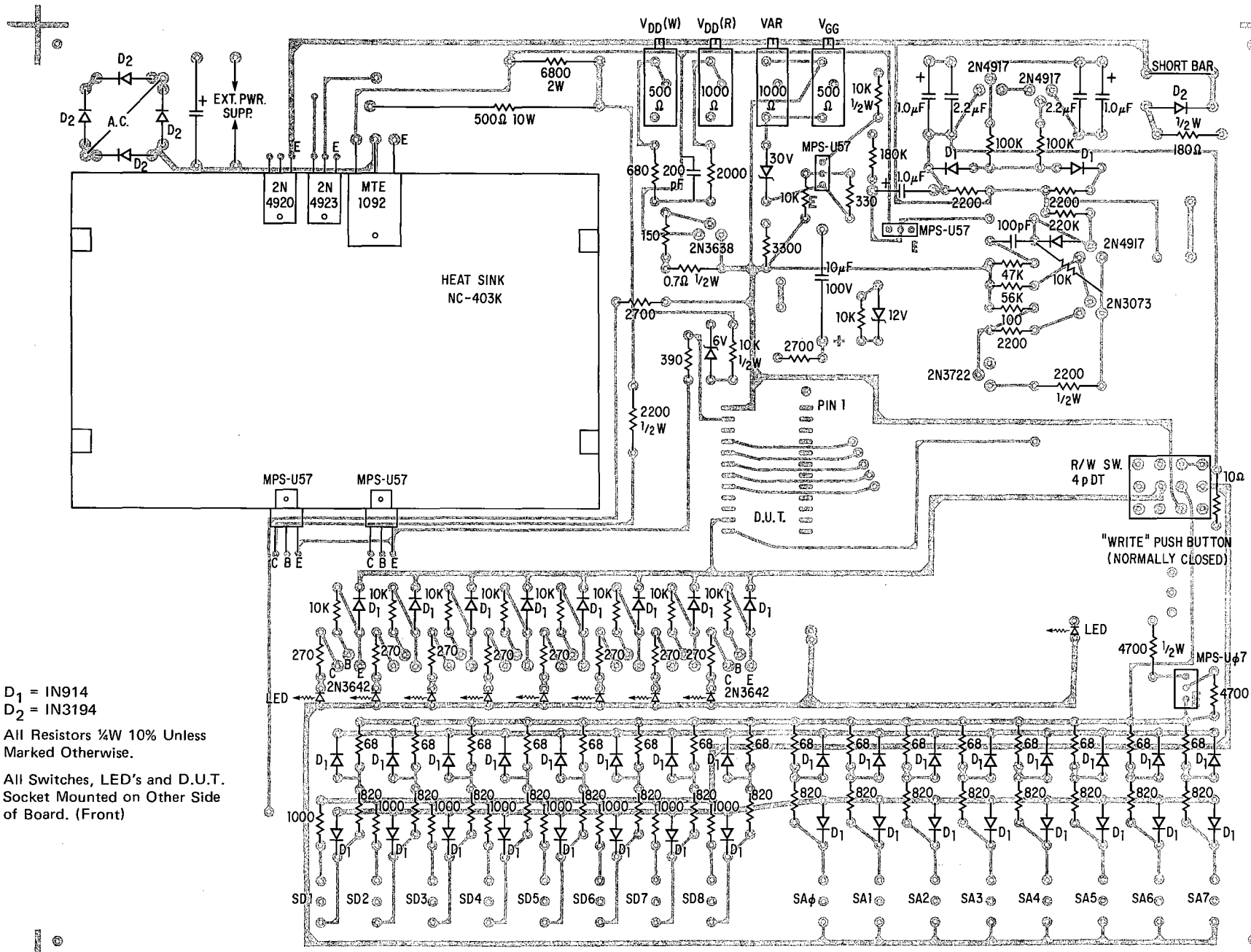
Miscellaneous	Quantity
Heat Sink NC403K	1 ea.
24 pin test socket	1 ea.
60-80V 1 amp Power Supply	1 ea.
P.C. Board (optional)	1 ea.



FRONT OF MANUAL PROGRAMMING ROM PC BOARD

SCALE: 65% OF ACTUAL BOARD SIZE

NOTE:
Only Switches, LED's and D.U.T.
Socket Mounted on This Side.



D_1 = IN914
D_2 = IN3194

All Resistors ¼W 10% Unless Marked Otherwise.

All Switches, LED's and D.U.T. Socket Mounted on Other Side of Board. (Front)

BACK OF MANUAL PROGRAMMING ROM PC BOARD
SCALE: 80% OF ACTUAL BOARD SIZE

Programming Instructions For Manual Programmer

1. Insert the device into the socket.
2. Turn on power.
3. Set the read/write, 4PDT switch ($S1_A$ through $S1_D$) to the W(Write) position.
4. Check for shorts in the data and address input pins by depressing the "write" push button and monitoring shorts indicator. If the indicator is flashing, attempts at writing should be discontinued until the problem is located. The first thing to be checked is to insure that the device has been correctly inserted in the socket.
5. Set the address inputs (toggle switches S_{A0} through S_{A7}) to the desired address (generally starting with address 00000000). The correct position for Logic "0" and Logic "1" is shown in the schematic.
6. Set the data inputs (toggle switches S_{D1} through S_{D7}) to the desired inputs for the selected address. The correct position for the Logic "0" and Logic "1" for the data input switches is shown in the schematic.
7. Then press the write push button and hold it for at least 5 seconds. Data has now been written.
8. To verify the data, set the read/write 4PDT switch to the R(Read) position. The data that has been written into the selected address will then be displayed on the LED's. A Logic "1" will be represented by a lit LED. A Logic "0" will be represented by a blank LED.
9. To write the next word, set the read/write, 4PDT switch to the W position and repeat steps 5 through 8.
10. The remaining words are then written into the device following the outlined sequence until the device is completely written into.

III. PROGRAMMING OF 1601/1701 AND 1602/1702 USING INTEL 7600 PROGRAMMER.

The 1601/1701 and 1602/1702 have been designed to facilitate rapid turnaround of custom patterns. Patterns supplied on paper tape are electrically programmed into the ROM by the 7600 programmer. Programmers are located at Intel, major distributors, and at many of our representatives in the U.S., Europe, and Japan. Programmers will also be available for sale to customers.

Programmer Description

The paper tape containing the custom pattern is loaded into the programmer which verifies the format and length of the data field. After loading, the programmer will write the data from the paper tape into the ROM (1601, 1701, 1602, or 1702).

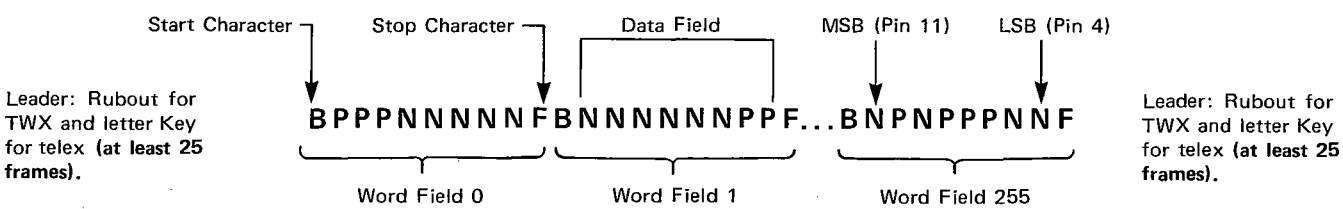
To insure that the ROM has been properly programmed, it is read out for every address and compared with the data of the paper tape. Reading is done in both the dynamic and static mode. An error will stop the read cycle at the bad word location. The displays on the programmer will indicate the bad word location and the 8 output bits of the ROM. For comparison the 8 input bits are also displayed.

A 1601, 1701, 1602, or 1702 is loaded again into the programmer and the programming cycle is repeated.

Tape Format

The 7600 programmer accepts 1" wide paper tape using 7 or 8 bit ASCII code, such as a model 33 ASR teletype produces. These programmers can also be used with the narrower 5 bit Telex tape. For such a tape to correctly program a 1601/1701 or 1602/1702, it must follow exactly the format rules below.

The format required by the 7600 is as shown below:



NOTE: Intel cannot assume responsibility for the programming circuit described in this data sheet.

ERRATA SHEET

(To replace Programming Instructions for Manual Programmer given on the top of Page 18 of the 1601/1701, 1602/1702, 1301 Data Sheet)

PROGRAMMING INSTRUCTIONS FOR MANUAL PROGRAMMER

1. Insert the device into the socket.
2. Turn on power
3. Set the read/write, 4PDT switch ($S1_A$ through $S1_D$) to the W (Write) position.
4. Set the address inputs (toggle switches S_{A0} through S_{A7}) to the desired address (generally starting with address 00000000). The correct position for Logic "0" and Logic "1" is shown in the schematic.
5. Set the data inputs (toggle switches S_{D1} through S_{D7}) to the desired inputs for the selected address. The correct position for the Logic "0" and Logic "1" for the data input switches is shown in the schematic.
6. Then press the write push button and hold it for at least 5 seconds. Data has now been written.

   Note: If the shorts indicator begins to flash, writing should be discontinued until the problem is located. The first thing to be checked is to insure that the device has been correctly inserted in the socket.

7. To verify the data, set the read/write 4PDT switch to the R (Read) position. The data that has been written into the selected address will then be displayed on the LED's. A logic "1" will be represented by a lit LED. A Logic "0" will be represented by a blank LED.

8. To write the next word, set the read/write, 4PDT switch to the W position and repeat steps 5 through 8.

9. The remaining words are then written into the device following the outlined sequence until the device is completely written into.

The format requirements are as follows:

1. There must be exactly 256 word fields in consecutive sequence, starting with word field 0 (all address lines low — refer to the table shown on page 10).

2. Each word field must consist of 10 consecutive characters, the first of which must be the start character B. Following the start character, there must be exactly 8 data characters (P's or N's) and ending with the stop character F. NO OTHER CHARACTERS, SUCH AS RUBOUTS, ARE ALLOWED ANYWHERE IN A WORD FIELD. If in preparing a tape, an error is made, the entire word field, including the B and F, must be rubbed out. Within the word field, a P results in a high level output, an N results in a low level output. The first data character corresponds to the desired output for data bit 8 (pin 11), the second for data bit 7 (pin 10), etc.

3. Preceding the first word field and following the last word field, there must be a leader/trailer length of at least 25 characters. This should consist of rubout punches (letter key for Telex tapes).

4. Between word fields, comments **not containing B's or F's** may be inserted. It is recommended that carriage return and line feed characters be inserted (as a "comment") just before each word field or at least between every four word fields. When these carriage returns, etc., are inserted, the tape may be easily listed on the teletype for purposes of error checking. The customer may also find it helpful to insert the word number (as a comment) at least every four word fields.

5. Included in the tape before the leader should be the customers complete Telex or TWX number and if more than one pattern is being transmitted, the ROM pattern number.

INTEL Telex No.	346372
INTEL TWX No.	910-338-0026
Japan's Telex No.	26364
Europe Telex No.	21060

IV. PARALLEL PROGRAMMING OF 1601/1701 AND 1602/1702.

When programming several ROMs in parallel, $\overline{CS}$ and V_{CC} should be at 0V for all 1601/1701 or 1602/1702 while the program pulse is applied only to the ROM being programmed. Pulsed V_{DD} and V_{GG} may be applied to all ROMs (both selected and unselected chips). However, if V_{DD} and V_{GG} are individually decoded, so that V_{DD} and V_{GG} are applied only to the ROM being programmed, multiplexing techniques may be used to permit programming an entire array in the same time that one part is programmed.

V. MASK PROGRAMMING OF 1301.

Tape Format

The custom patterns may be sent in on a Telex or submitted as a paper tape in a 7 or 8 bit ASCII code from model 33 teletype or TWX. The paper tape format is exactly the same as for the 1601/1701 and 1602/1702.

Truth Table

The custom patterns may be sent in on a truth table. Blank custom truth table forms are available upon request from Intel.

VI. 1701, 1702 ERASING PROCEDURE.

The 1701 and 1702 may be erased by exposure to a high intensity ultraviolet light source. A 1701 or 1702 placed 1 to 1.5 inches from a light source with an ultraviolet wavelength of 2537Å at an intensity of 10 mW/cm^2 (i.e. a dosage of 6W sec/cm^2) will be erased in 10 minutes. An example of a light source which is capable of producing the required ultraviolet wavelength and intensity is the Model R51 manufactured by Ultraviolet Products (San Gabriel, California).

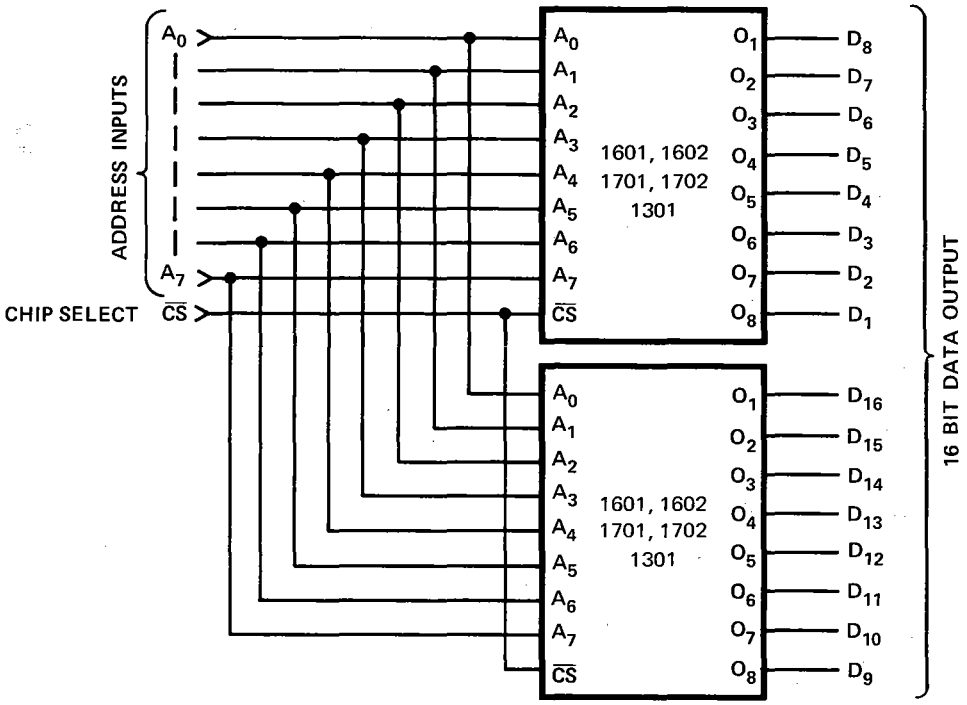
Application Information

POWER DISSIPATION CONSIDERATIONS

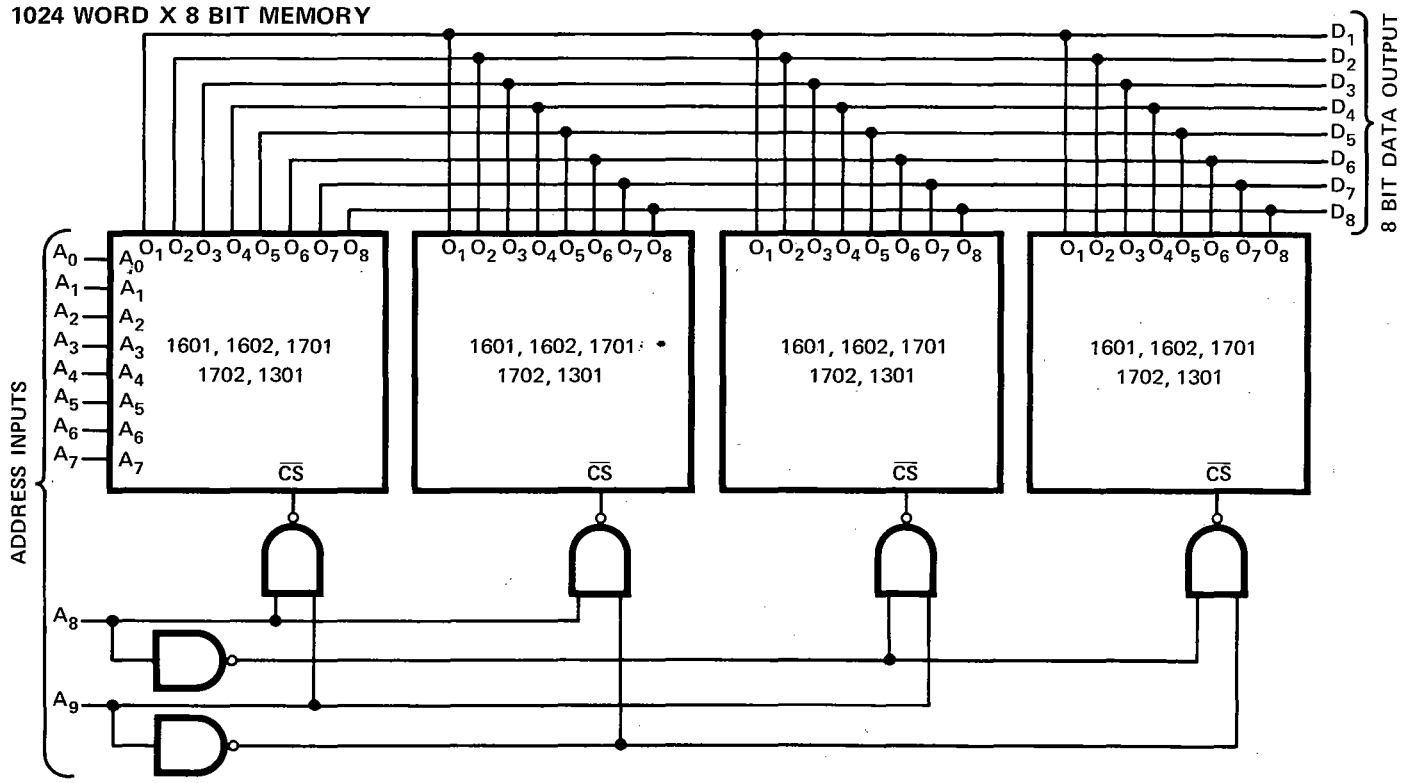
Peak power dissipation in the dynamic mode occurs when the ϕ_1 clock is low. At other times, two sources of power dissipation must be considered: A fixed current flow (from V_{CC} to V_{DD}) which corresponds to I_{DDO}, and the current flowing through the output terminals. These output currents continue to flow after the end of the cycle. To prevent these currents from flowing when the memory is inactive (yet has V_{DD} applied), the chip must be deselected before the clocks are deactivated. Deselection can be accomplished only by executing a memory cycle with $\overline{CS}$ in the deselect condition.

256 WORD BY 16 BIT ROM

In this example the 8 bit address bus A_0 - A_7 and $\overline{CS}$ lines are connected in parallel. A full 16 bit word is made up of 8 bits from each 1601/1701, 1602/1702 and 1301 package.



1024 WORD X 8 BIT MEMORY



INTEL CORP. 3065 Bowers Avenue, Santa Clara, California 95051 • (408) 246-7501

Printed in U.S.A.

7136/1