2K (256 x 8) UV ERASABLE LOW POWER PROM

Part No.	MAXIMUM ACCESS (μs)	t_{DVGG} (μs)
1702AL	1.0	0.4
1702AL-2	0.65	0.3

- **Clocked V_{GG} Mode for Low Power Dissipation**
- **Fast Programming: 2 Minutes for all 2048 Bits**
- **All 2048 Bits Guaranteed* Programmable: 100% Factory Tested**
- **Inputs and Outputs DTL and TTL Compatible**
- **Three-State Output: OR-tie Capability**

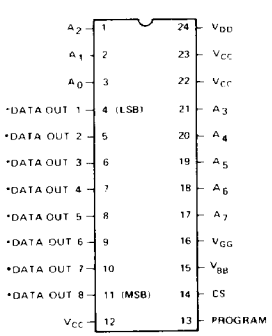
The 1702AL is a 256 word by 8 bit electrically programmable ROM and is the same chip as the industry standard 1702A. The programming and erasing specifications are identical to the 1702A. The 1702AL operates with the V_{GG} clocked to reduce the power dissipation.

Initially all 2048 bits of the 1702AL are in the "0" state (output low). Information is introduced by selectively programming "1"s (output high) in the proper bit location. The 1702AL is packaged in a 24 pin dual in-line package with a transparent lid. The transparent lid allows the user to expose the 1702AL to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device.

The 1702AL is fabricated with silicon gate technology. This low threshold technology allows the design and production of high performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

*Intel's liability shall be limited to replacing any unit which fails to program as desired.

PIN CONFIGURATION

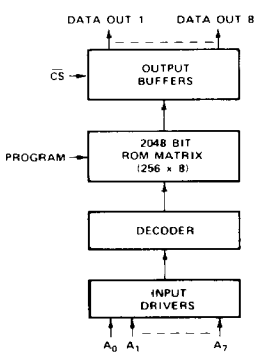


*THIS PIN IS THE DATA INPUT LEAD DURING PROGRAMMING

PIN NAMES

A_0–A_7	Address Inputs
$\overline{CS}$	Chip Select Input
D_{OUT1}–D_{OUT8}	Data Outputs

BLOCK DIAGRAM



NOTE: In the read mode a logic 1 at the address inputs and data outputs is a high and logic 0 is a low.

U.S. Patent No. 3660819

PIN CONNECTIONS

The external lead connections to the 1702AL differ, depending on whether the device is being programmed or used in read mode (see following table). In the programming mode, the data inputs 1-8 are pins 4-11 respectively. *The programming voltages and timing are shown in the Data Catalog ROM and PROM Programming Instructions section.*

MODE \ PIN	12 (V_{CC})	13 (Program)	14 (CS)	15 (V_{BB})	16 (V_{GG})	22 (V_{CC})	23 (V_{CC})	24 (V_{DD})
Read	V_{CC}	V_{CC}	GND	V_{CC}	Clocked V_{GG}	V_{CC}	V_{CC}	V_{DD}
Programming	GND	Program Pulse	GND	V_{BB}	Pulsed V_{GG}	GND	GND	Pulsed V_{DD}

Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . -10°C to +80°C
Storage Temperature . . . . . −65°C to +125°C
Soldering Temperature of Leads (10 sec) . . . . . +300°C
Power Dissipation . . . . . 2 Watts
Read Operation: Input Voltages and Supply
Voltages with respect to V_{CC} . . . . . +0.5V to −20V
Program Operation: Input Voltages and Supply
Voltages with respect to V_{CC} . . . . . −48V

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{CC} = +5V ±5%, V_{DD} = -9V ±5%, V_{GG}[1] = -9V ±5%, unless otherwise noted.

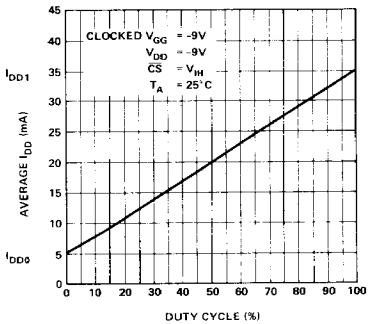
READ OPERATION

Symbol	Test	1702AL Limits Min.	Typ.[2]	Max.	1702AL-2 Limits Min.	Typ.[2]	Max.	Unit	Conditions
I_{LI}	Address and Chip Select Input Load Current			1			1	μA	V_{IN} = 0.0V
I_{LO}	Output Leakage Current			1			1	μA	V_{OUT} = 0.0V, $\overline{CS}$ = V_{CC}-2
I_{DDO1}[1]	Power Supply Current		7	10		7	10	mA	T_A=25°C $\overline{CS}$=V_{IH}, V_{GG}=V_{CC},
I_{DDO2}	Power Supply Current			15			15	mA	T_A=0°C I_{OL}=0.0mA
I_{DD1}[1]	Power Supply Current		35	50		35	50	mA	$\overline{CS}$ = V_{CC} -2, I_{OL} = 0.0mA, T_A = 25°C, Continuous
I_{DD2}	Power Supply Current		32	46		32	46	mA	$\overline{CS}$ = 0.0V, I_{OL} = 0.0mA, T_A = 25°C, Continuous
I_{DD3}	Power Supply Current		38	60		38	60	mA	$\overline{CS}$ = V_{CC} -2, I_{OL} = 0.0mA, T_A = 0°C, Continuous
I_{CF1}	Output Clamp Current		8	14		5.5	8	mA	V_{OUT} = -1.0V, T_A = 0°C, Continuous
I_{CF2}	Output Clamp Current		7	13		5	7	mA	V_{OUT} = -1.0V, T_A = 25°C, Continuous
I_{GG}	Gate Supply Current			1			1	μA	
V_{IL1}	Input Low Voltage for TTL Interface	-1		0.65	-1		0.65	V	
V_{IL2}	Input Low Voltage for MOS Interface	V_{DD}		V_{CC}-6	V_{DD}		V_{CC}-6	V	
V_{IH}	Address and Chip Select Input High Voltage	V_{CC}-2		V_{CC}+0.3	V_{CC}-2		V_{CC}+0.3	V	
I_{OL}	Output Sink Current	1.6	4		1.6	4		mA	V_{OUT} = 0.45V
I_{OH}	Output Source Current	-2.0			-2.0			mA	V_{OUT} = 0.0V
V_{OL}	Output Low Voltage		-3	0.45		-3	0.45	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage	3.5	4.5		3.5	4.5		V	I_{OH} = -200μA

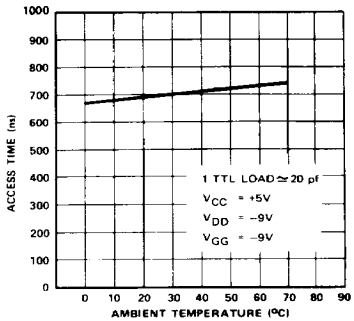
NOTES: 1. The 1702AL is operated with the V_{GG} clocked to obtain low power dissipation. The average I_{DD} will vary between I_{DD0} and I_{DD1} (at 25°C) depending on the V_{GG} duty cycle (see curve opposite). 2. Typical values are at nominal voltage and T_A = 25°C.

TYPICAL CHARACTERISTICS

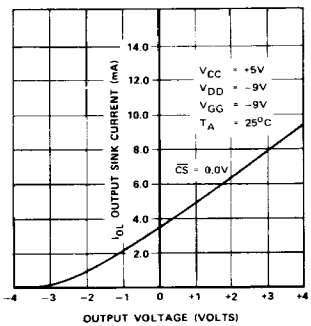
AVERAGE CURRENT VS. DUTY CYCLE FOR CLOCKED V_{GG}



ACCESS TIME VS. TEMPERATURE



OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



PROM/ROM

A.C. CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$, $V_{DD} = -9V \pm 5\%$ unless otherwise noted

Symbol	Test	1702AL Limits Min.	1702AL Limits Max.	1702AL-2 Limits Min.	1702AL-2 Limits Max.	Unit
Freq.	Repetition Rate		1		1.6	MHz
t_{ACC}	Address to output delay		1		0.65	μs
t_{DVGG}	Clocked V_{GG} set up	0.4		0.3		μs
t_{CS}	Chip select delay		0.1		0.3	μs
t_{CO}	Output delay from $\overline{CS}$		0.9		0.35	μs
t_{OD}	Output deselect		0.3		0.3	μs
t_{OHC}	Data out hold in clocked V_{GG} mode		5		5	μs

CAPACITANCE $T_A = 25°C$

SYMBOL	TEST	TYPICAL	MAXIMUM	UNIT	CONDITIONS
C_{IN}	Input Capacitance	8	15	pF	$V_{IN} = V_{CC}$, $\overline{CS} = V_{CC}$, $V_{OUT} = V_{CC}$, $V_{GG} = V_{CC}$ — All unused pins are at A.C. ground
C_{OUT}	Output Capacitance	10	15	pF	
$C_{V_{GG}}$	V_{GG} Capacitance (Note 1)		30	pF	

*This parameter is periodically sampled and is not 100% tested.

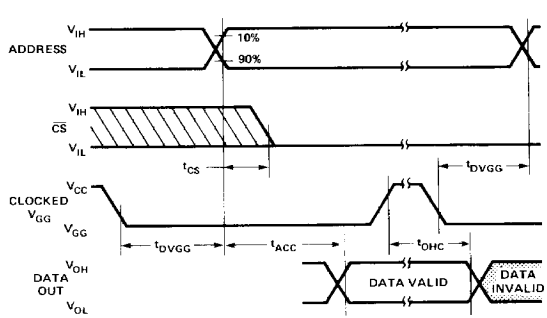
SWITCHING CHARACTERISTICS

Conditions of Test:

Input pulse amplitudes: 0 to 4V; t_R, $t_F \leqslant 50$ ns

Output load is 1 TTL gate; measurements made at output of TTL gate ($t_{PD} \leqslant 15$ ns), $C_L = 15pF$

A. READ OPERATION



B. DESELECTION OF DATA OUTPUT IN OR-TIE OPERATION