1702A-I

DESCRIPTION

The 1702A is ideally suited for uses where fast turn-around and pattern experimentation are important. The device undergoes complete programming and functional testing on each bit position prior to shipment, thus insuring 100% programmability.[1]

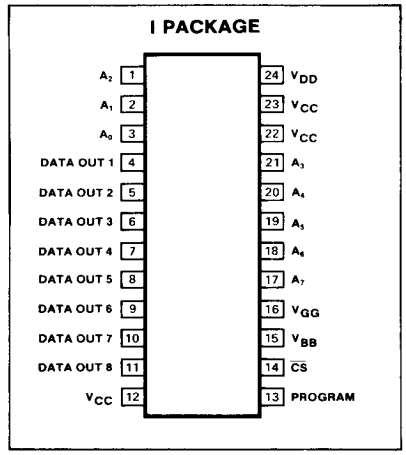
The 1702A is packaged in a 24-pin dual in-line package with a UV transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device.

The 1702A is fabricated with silicon gate technology. This low threshold technology allows the design and production of high performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

FEATURES

- **Fast programming for all 2048 bits: 2 minutes**
- **All 2048 bits guaranteed programmable**
- **100% factory tested**
- **Fully decoded**
- **Static MOS: No clocks required**
- **Inputs and outputs DTL and TTL compatible**
- **Tri-state output: OR-tie capability**
- **Simple memory expansion**
- **Chip select input lead**

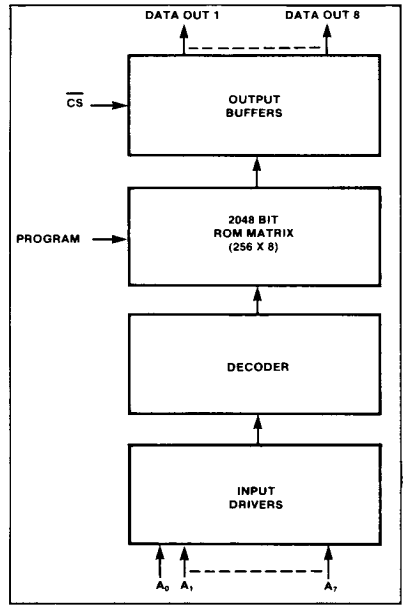
PIN CONFIGURATION



PIN DESIGNATION[2]

PIN NO.	SYMBOL	NAME & FUNCTION
		Read mode
12	V_{CC}	V_{CC}
13	Program	V_{CC}
14	$\overline{CS}$	GND
15	V_{BB}	V_{CC}
16	V_{GG}	V_{GG}
22	V_{CC}	V_{CC}
23	V_{CC}	V_{CC}
		Programming mode
12	V_{CC}	GND
13	Program	Program pulse
14	$\overline{CS}$	GND
15	V_{BB}	V_{BB}
16	V_{GG}	Pulsed V_{GG} (V_{IL4P})
22	V_{CC}	GND
23	V_{CC}	GND

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[3]

PARAMETER		RATING	UNIT
	Temperature range		°C
T_A	Operating	0 to +70	
T_{STG}	Storage	-65 to +125	
P_D	Power dissipation	2	W
	Soldering of leads (10sec)	300	°C
	Input voltages and supply voltages with respect to V_{CC}		V
	Read operation	0.5 to -20	
	Program operation	-48	

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{DD} = -9V ± 5%, V_{GG}[3] = -9V ± 5% unless otherwise specified.[4]

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					V
V_{IL1}	Low for TTL interface		-1.0		0.65	
V_{IL2}	Low for MOS interface		V_{DD}		V_{CC}-6	
V_{IH}	Address and chip select high		V_{CC}-2		V_{CC}+0.3	
	Output voltage					V
V_{OL}	Low	I_{OL} = 1.6mA		-.7	0.45	
V_{OH}	High	I_{OH} = -100μA	3.5	4.5		
I_{LI}	Address and chip select input load current	V_{IN} = 0.0V			1	μA
I_{LO}	Output leakage current	V_{OUT} = 0.0V, $\overline{CS}$ = V_{CC} -2			1	μA
	Supply current	I_{OL} = 0.0mA				mA
I_{DD1}		$\overline{CS}$ = V_{CC} -2, T_A = 25°C		35	50	
I_{DD2}		$\overline{CS}$ = 0.0, T_A = 25°C		32	46	
I_{DD3}		$\overline{CS}$ = V_{CC} -2, T_A = 0°C		38.5	60	
I_{GG}	Gate				1	
	Output current					mA
	Clamp	V_{OUT} = -1.0V				
I_{CF1}		T_A = 0°C		8	14	
I_{CF2}		T_A = 25°C			13	
I_{OL}	Sink	V_{OUT} = 0.45V	1.6	4		
I_{OH}	Source	V_{OUT} = 0.0V	-2.0			
	Capacitance[5]	All unused pins are at ac ground				pF
C_{IN}	Input	V_{IN} = V_{CC}, $\overline{CS}$ = V_{CC}		8	15	
C_{OUT}	Output	V_{OUT} = V_{CC}, V_{GG} = V_{CC}		10	15	

AC ELECTRICAL CHARACTERISTICS

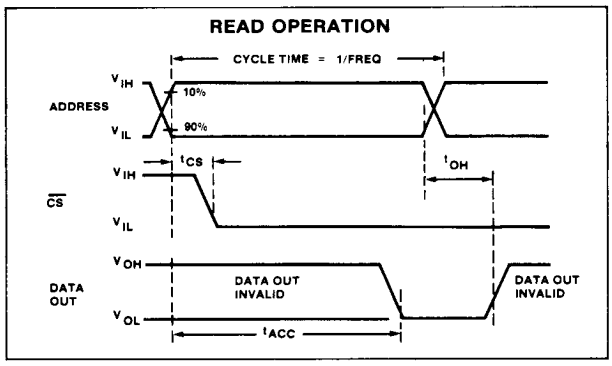
T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{DD} = -9V ± 5% unless otherwise specified, Input pulse amplitudes = 0 to 4V, t_R, $t_F \leq$ 50ns, Output load is 1 TTL gate, Measurements made at output of TTL gate ($t_{PD} \leq$ 15ns), C_L = 15pF

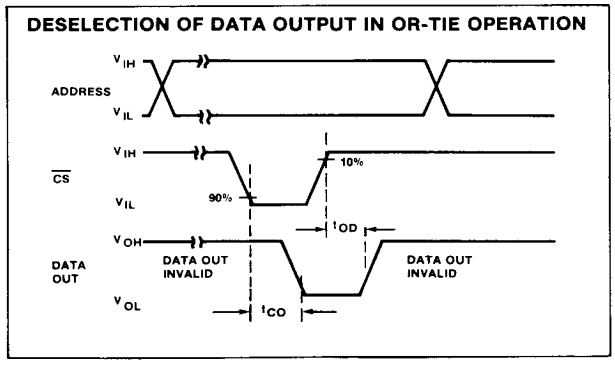
PARAMETER		TO	FROM	LIMITS			UNIT
				Min	Typ	Max	
Freq	Repetition Rate					1	MHz
t_{OH}	Previous read data valid					100	ns
	Delay time						
t_{ACC}[1]		Output	Address		0.7	1	μs
t_{CS}		Output	Chip select $\overline{CS}$			100	ns
t_{CO}		Output				900	ns
t_{OD}	Output deselect					300	ns

NOTES

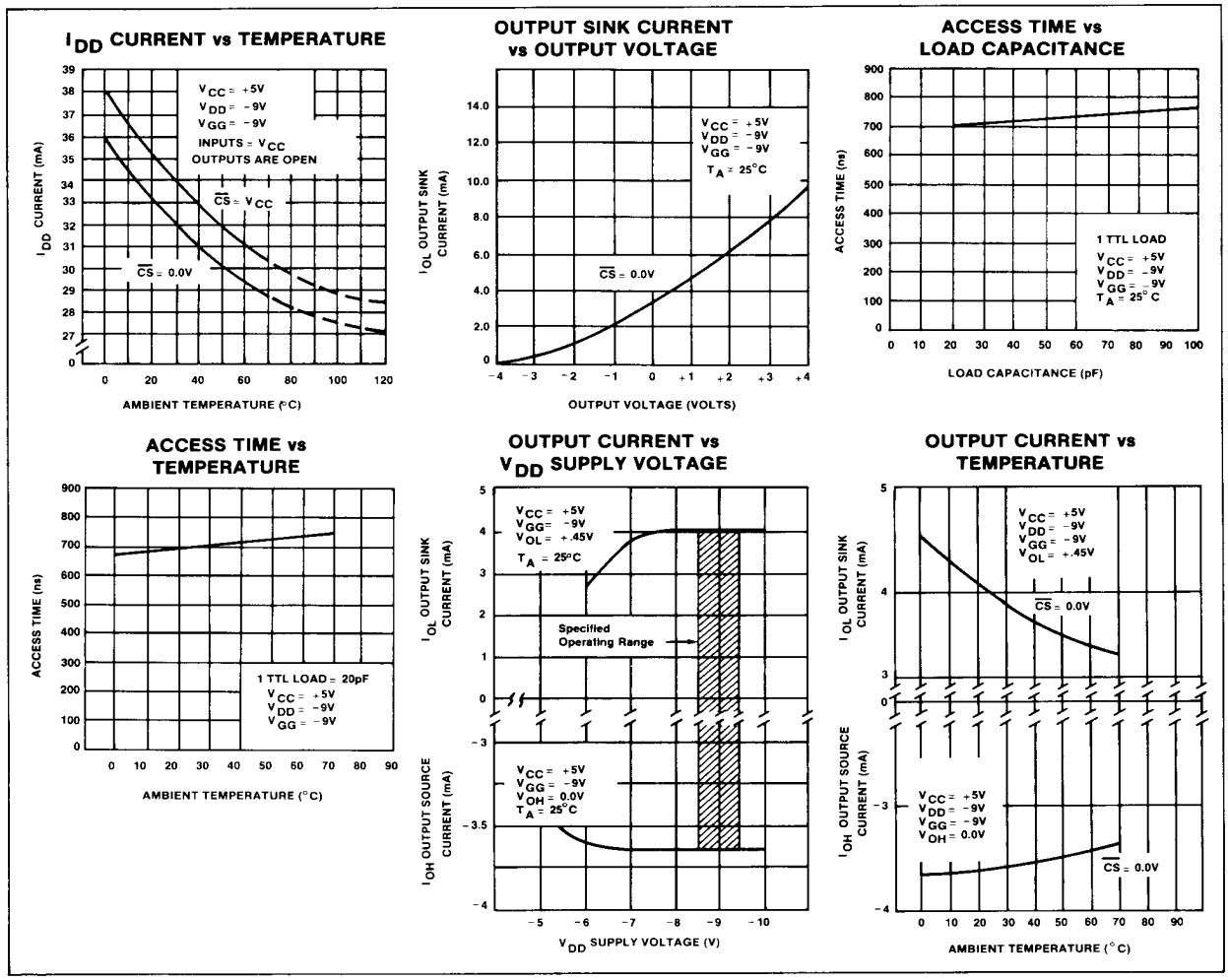
1. Signetics liability shall be limited to replacing any unit which fails to program as desired.
2. The external lead connections to the 1702A differ depending on whether the device is being programmed or used in read mode. In the programming mode, the data inputs 1-8 are pins 4-11 respectively.
3. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
4. Typical values are T_A = 25°C and at typical supply voltages.
5. This parameter is perdiodically sampled and is not 100° tested.

TIMING DIAGRAMS





TYPICAL PERFORMANCE CHARACTERISTICS



DC AND OPERATING PROGRAMMING CHARACTERISTICS

T_A = 25°C, V_{CC} = 0V, V_{BB} = +12V ± 10%, $\overline{CS}$ = 0V unless otherwise specified.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					V
V_{IHP}	High			0.3		
V_{IL1P}	Pulsed data low		-46	-48		
V_{IL2P}	Address low		-40	-48		
V_{IL3P}	Pulsed low V_{DD} and program		-46	-48		
V_{IL4P}	Pulsed low V_{GG}		-35	-40		
	Load current					mA
I_{LI1P}	Address and data input	V_{IN} = -48V		10		
I_{LI2P}	Program and V_{GG}	V_{IN} = -48V		10		
I_{BB}	V_{BB} supply[1]		10	100		
I_{DDP}	Peak I_{DD} supply[2]	V_{DD} = V_{prog} = -48V, V_{GG} = -35V	200	300		

AC PROGRAMMING CHARACTERISTICS

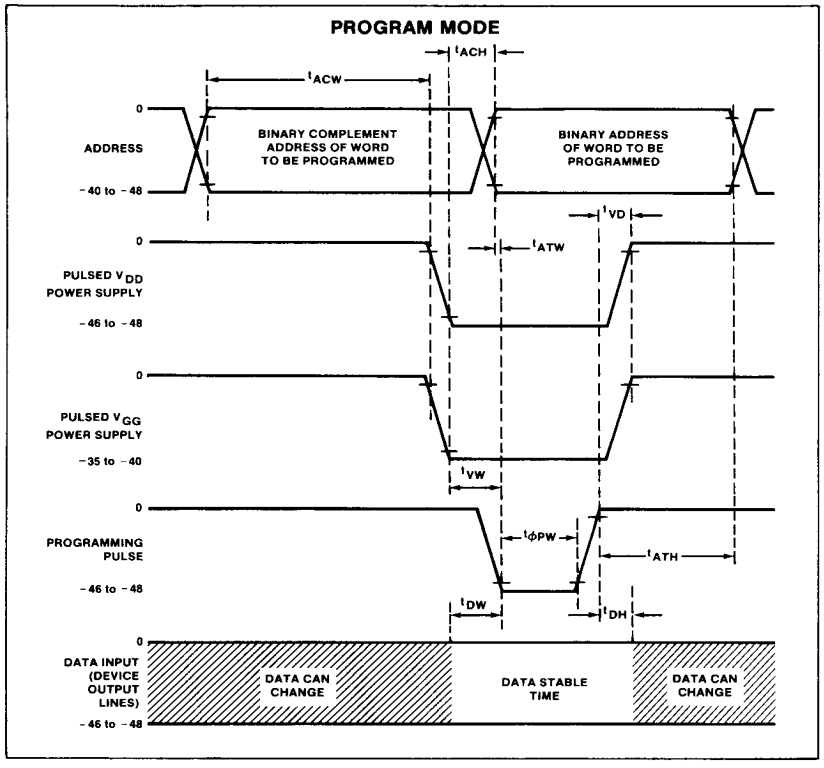
T_A = 25°C, V_{CC} = 0V, V_{BB} = +12V ± 10%, $\overline{CS}$ = 0V, unless otherwise specified, Input rise and fall times = < 1μs unless otherwise specified.

PARAMETER		TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
	Duty cycle (V_{DD}, V_{GG})						20	%
$t_{\phi PW}$	Program pulse width			V_{DD} = V_{prog} = -48V, V_{GG} = -35V			3	ms
	Setup and hold time							μs
t_{DW}	Setup time	Programming pulse	Data		25			
t_{DH}	Hold time	Data	Programming pulse		10			
t_{VW}	Setup time	Programming pulse	Pulsed power supply		100			
t_{VD}	Hold time	Pulsed power supply	Programming pulse		10		100	
t_{ACW}	Setup time[3]	Pulsed V_{DD} power supply	Address		25			
t_{ACH}	Hold time[3]	Address	Pulsed V_{DD} power supply		25			
t_{ATW}	Setup time	Programming pulse	Address		10			
t_{ATH}	Hold time	Address	Programming pulse		10			

NOTES

1. The V_{BB} supply must be limited to 100mA current to prevent damage to the device.
2. I_{DDP} flows only during V_{DD}, V_{GG} on time. I_{DDP} should not be allowed to exceed 300mA for greater than 100μs. Average power supply current I_{DDP} is typically 40mA at 20% duty cycle.
3. All 8 address bits must be in the complement state when pulsed V_{DD} and V_{GG} move to their negative levels. The addresses (0-255) must be programmed as shown in the timing diagram.

TIMING DIAGRAM



OPERATION IN PROGRAM MODE

Initially, all 2048 bits of the ROM are in the low state. Information is introduced by selectively programming high's in the proper bit locations.

Word Address selection is done by the same decoding circuitry used in the Read mode (see dc Electrical Characteristics table). All 8 address bits must be in the binary complement state when pulsed V_{DD} and V_{GG} move to their negative levels. The addresses must be held in their binary complement state of a minimum of 25μs after V_{DD} and V_{GG} have moved to the negative levels. The addresses must then make the transition to their true state a minimum of 10μs before the program pulse is applied.

The 8 output terminals are used as data inputs to determine the information pattern in the 8 bits of each word. A low data input level (-48V) will then program a "1" and a high data input level (ground) will leave a "0" (see dc and Operating Programming Characteristics table). All 8 bits of one word are programmed simultaneously by setting the desired bit information patterns on the data input terminals.

During the progamming, V_{GG}, V_{DD} and the program pulse are pulsed signals. We recommend the P+4P smart programming routine where P = the number of programming pulses for data to read true; P max = 256; and 4P = the number of over programming pulses applied.

ERASING PROCEDURE

The 1702A may be erased by exposure to high intensity short-wave ultraviolet light at a wavelength of 2537A°. The recommended integrated dose (i.e., UV intensity x exposure time) is 6W-sec/cm^2. Examples of ultraviolet sources which can erase the 1702A in 10 to 20 minutes are the Model UVS-54 and Model S-52 short-wave ultraviolet lamps manufactured by Ultra-Violet Products, Inc., 5114 Walnut Grove Avenue, San Gabriel, Ca. The lamps should be used without short-wave filters, and the 1702A to be erased should be placed about one inch away from the lamp tubes.